



Compal Confidential

KAWGO Schematics Document

AMD S1g1 / RS690MC / SB600

2009 / 04 / 09

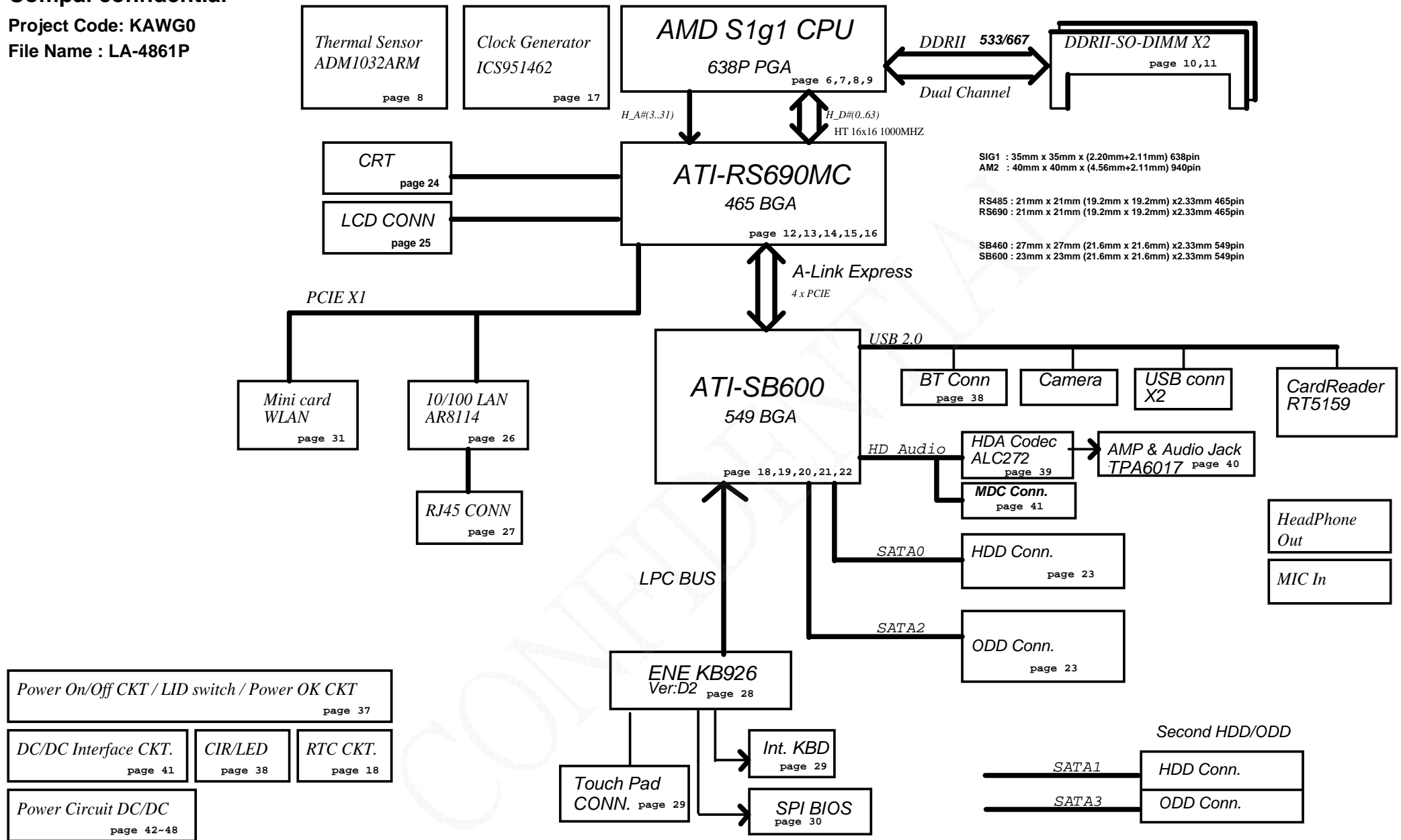
Rev:1.0

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		2009/06/11		Title	
				SCHEMATIC,MB A4861	
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				Rev	D

Compal confidential

Project Code: KAWG0

File Name : LA-4861P



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Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

External PCI Devices

EC SM Bus1 address EC SM Bus2 address

SB600 SM Bus 1 address SB600 SM Bus 2 address

SIGNAL STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

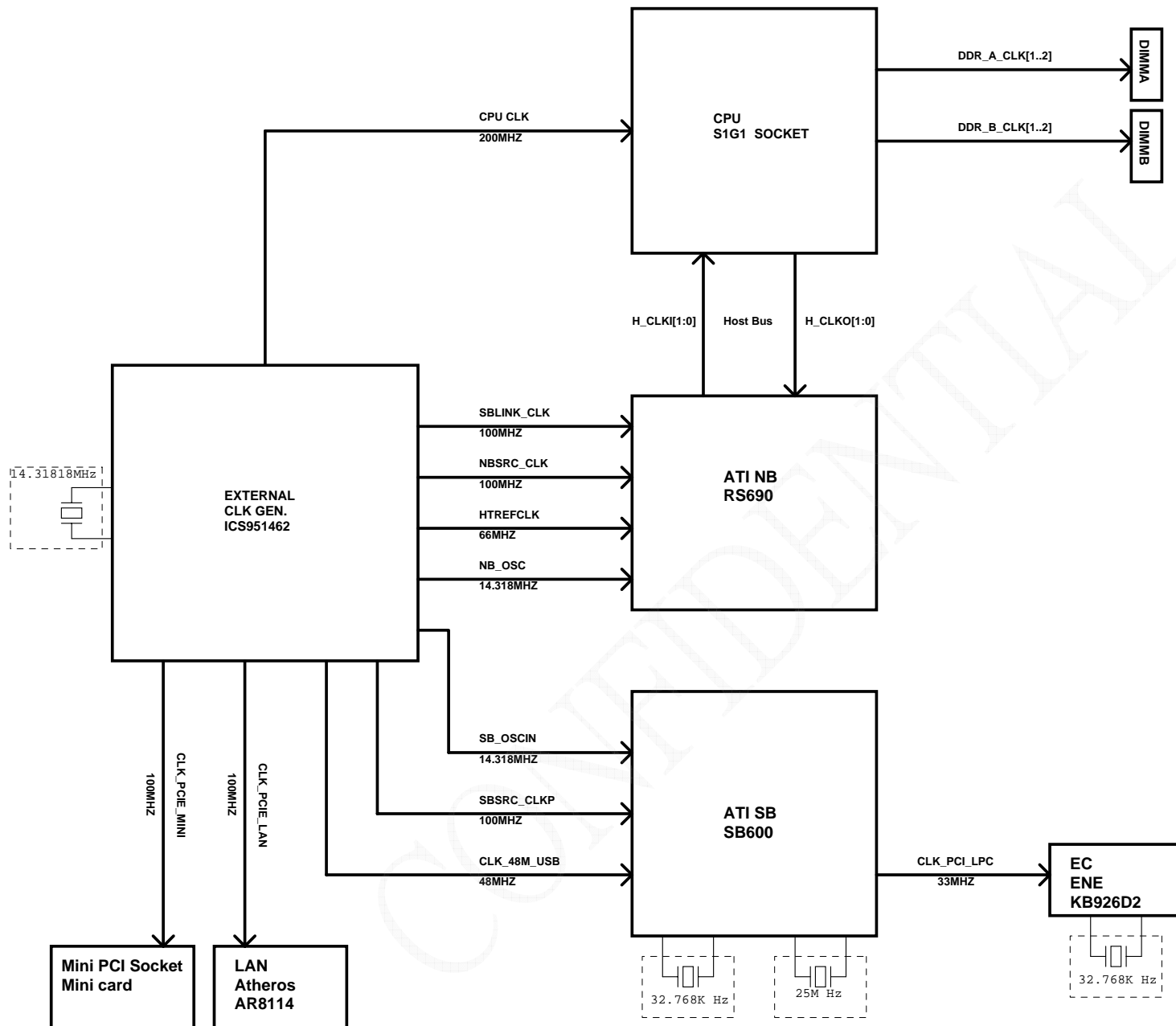
Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

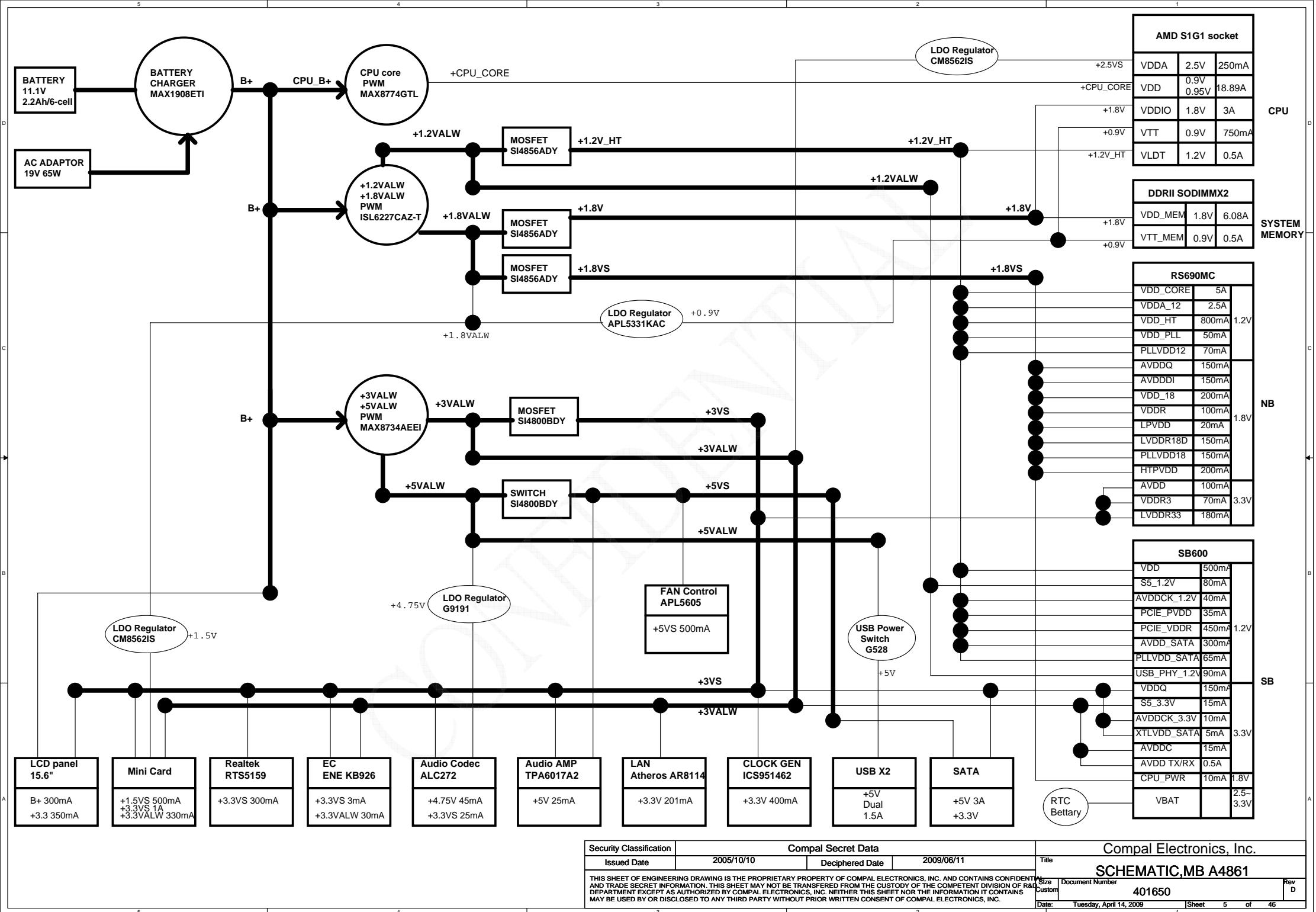
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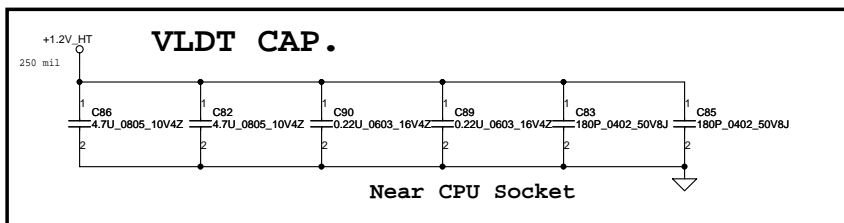
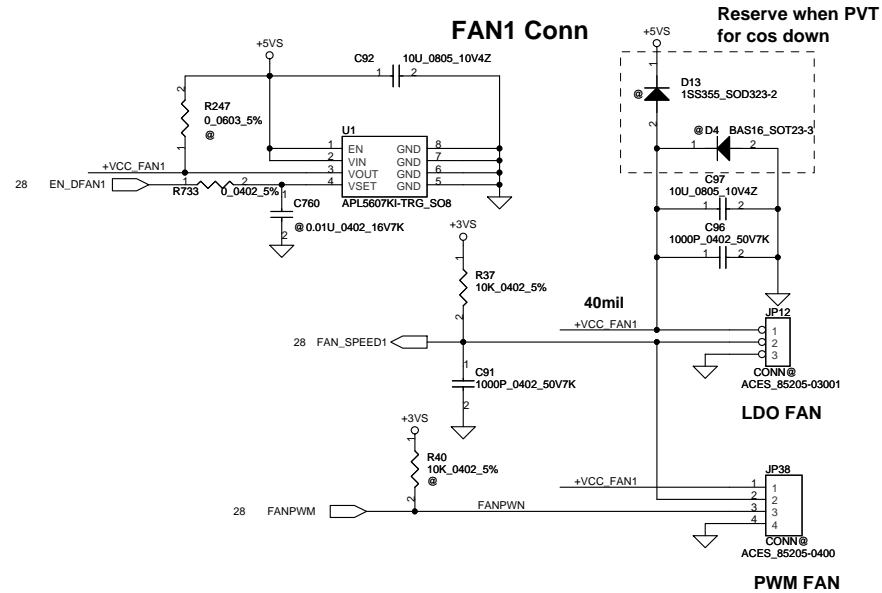
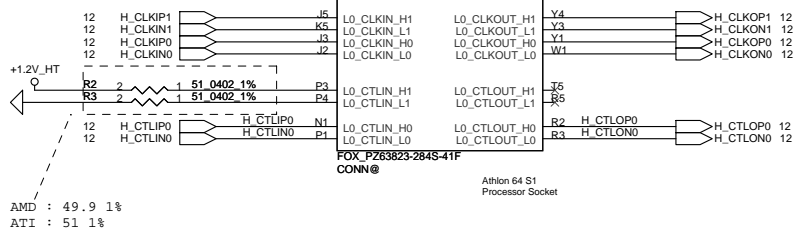
SKU ID	SKU
0	
1	
2	
3	
4	
5	
6	
7	

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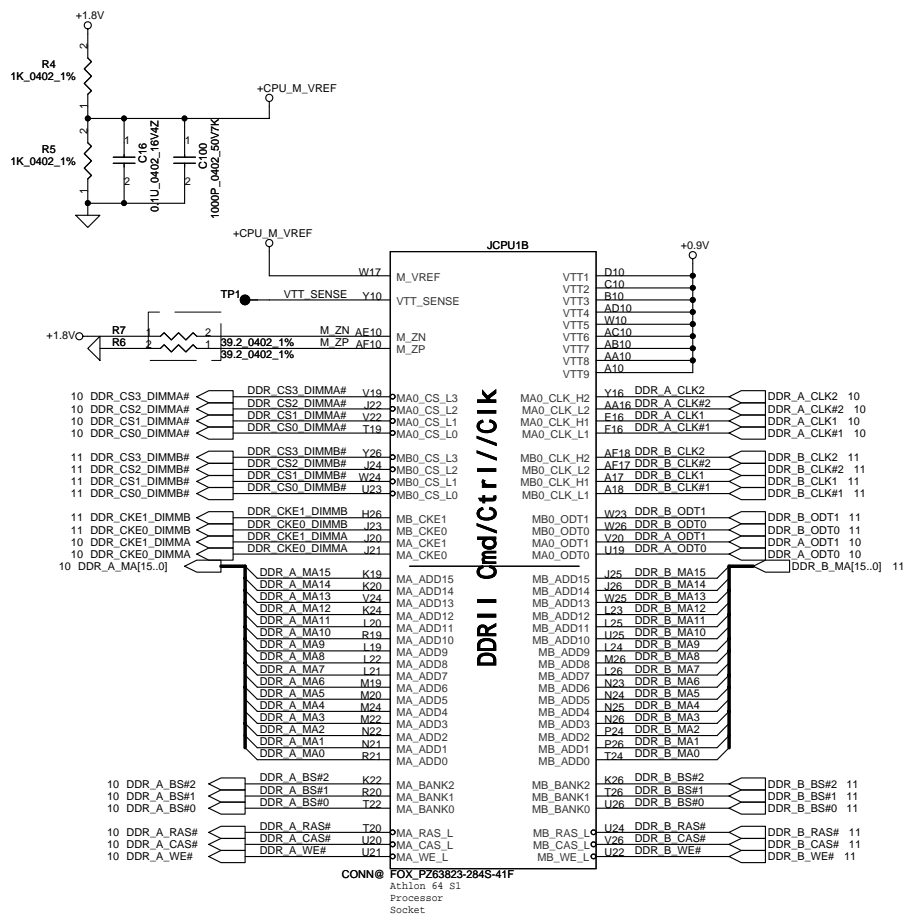


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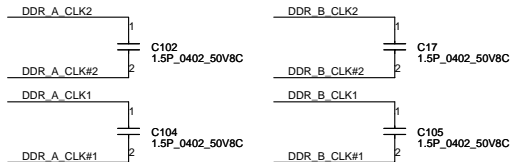




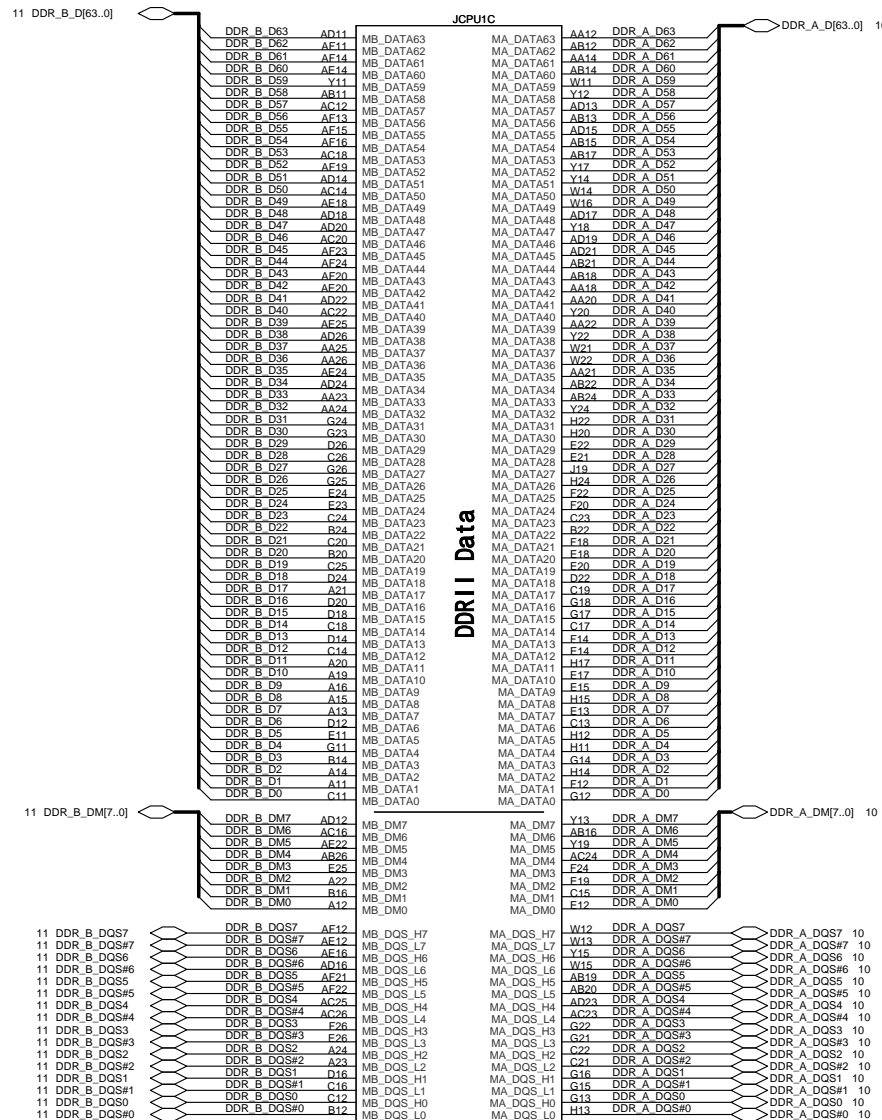
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PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

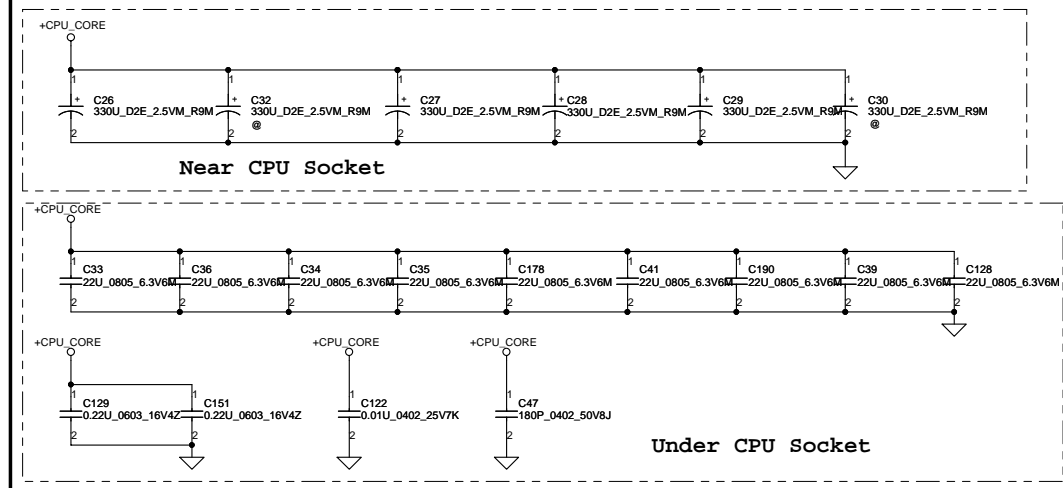


Processor DDR2 Memory Interface

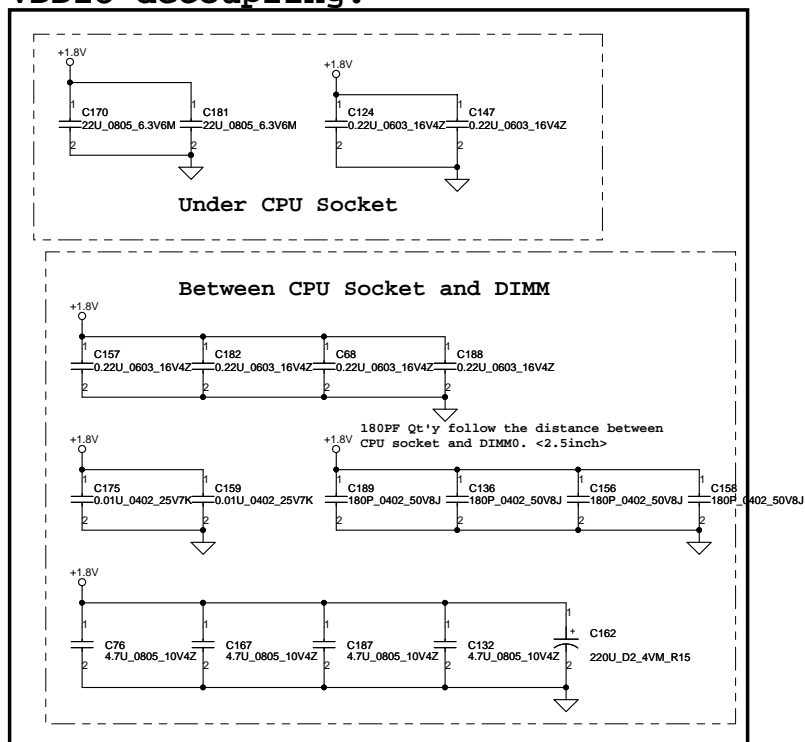


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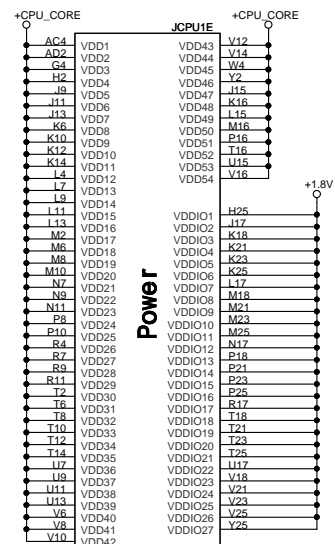
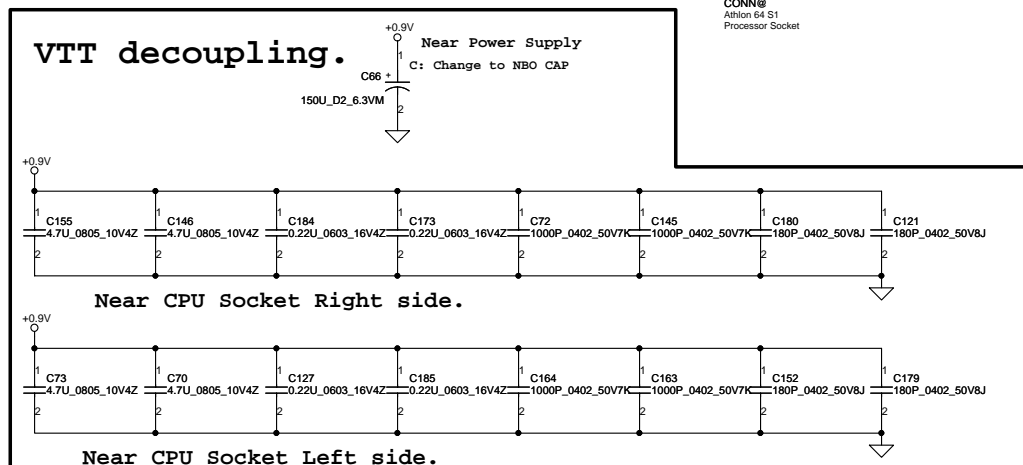
VDD(+CPU_CORE) decoupling.



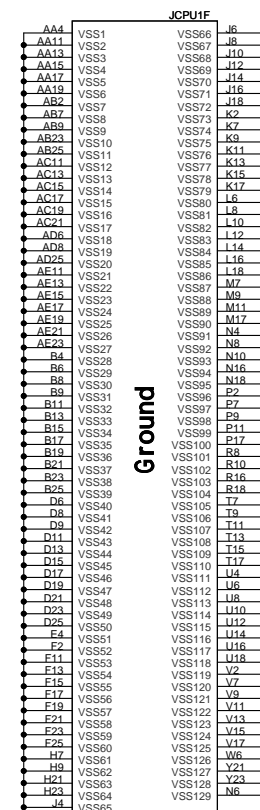
VDDIO decoupling.



VTT decoupling.



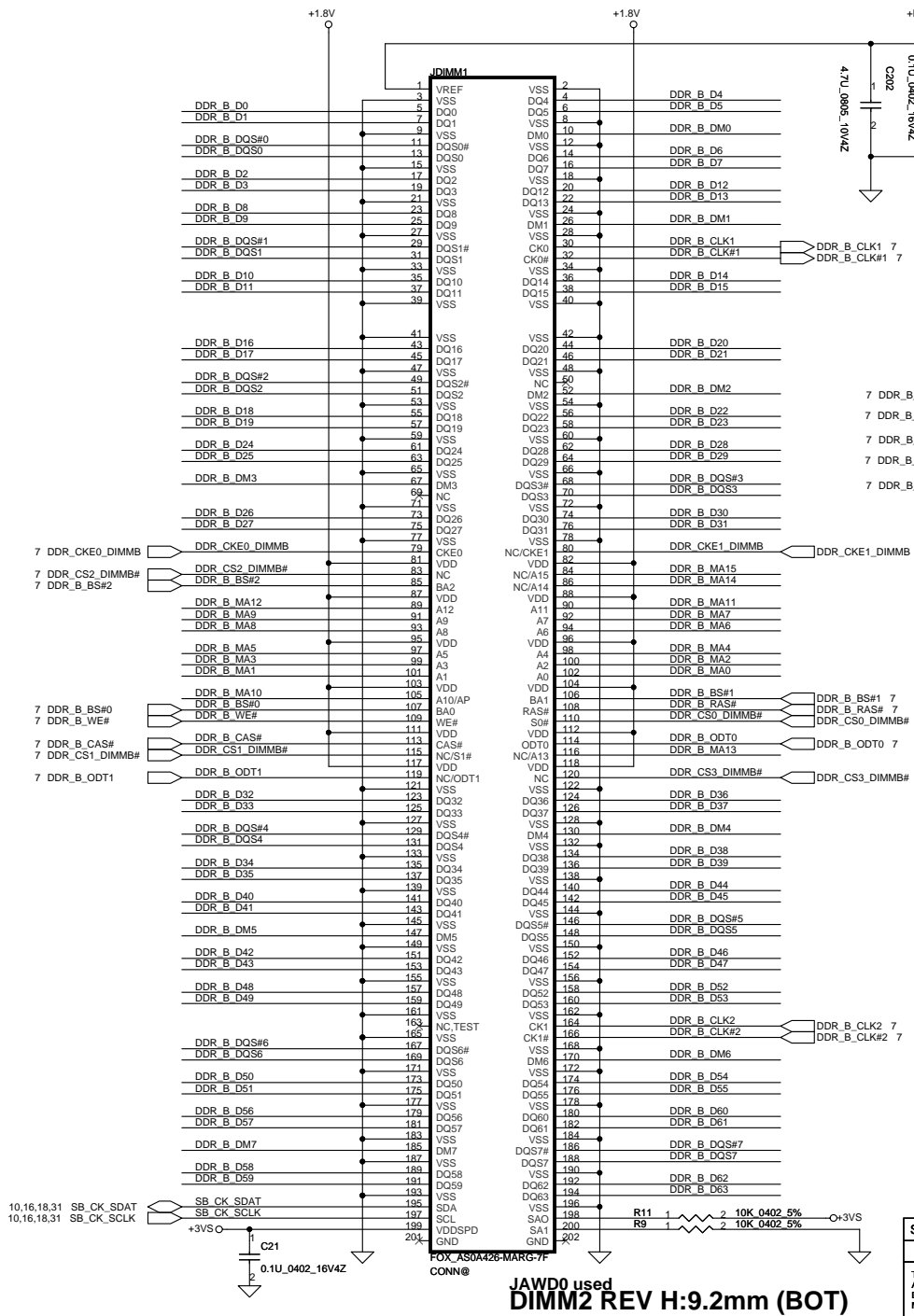
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CONN@
Athlon 64 S1
Processor Socket



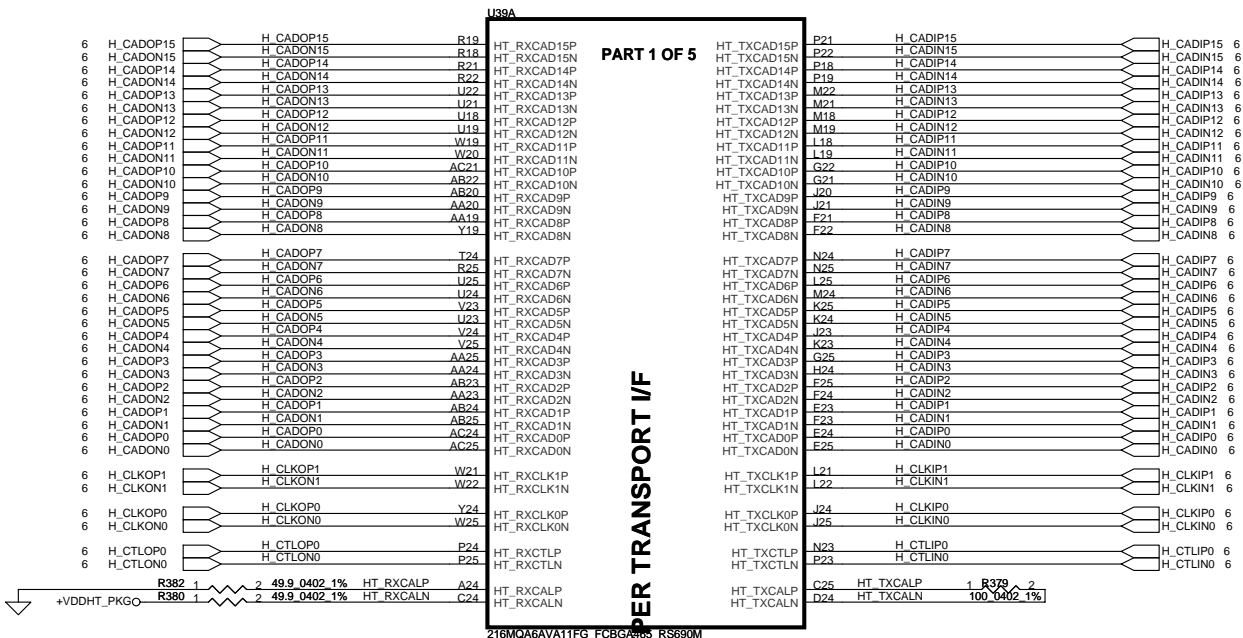
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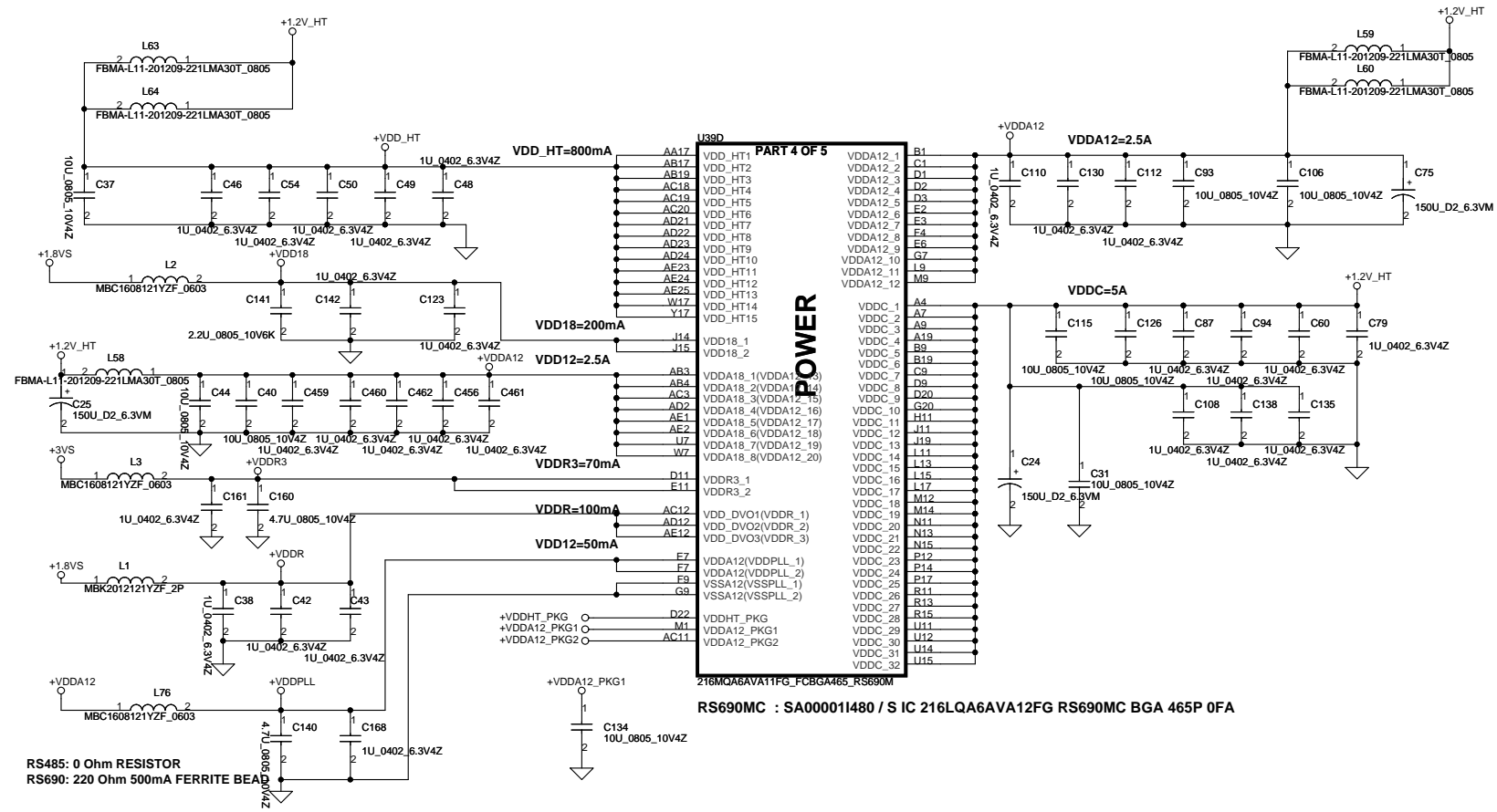
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RS690MC : SA000011480 / S IC 216LQA6AVA12FG RS690MC BGA 465P 0FA

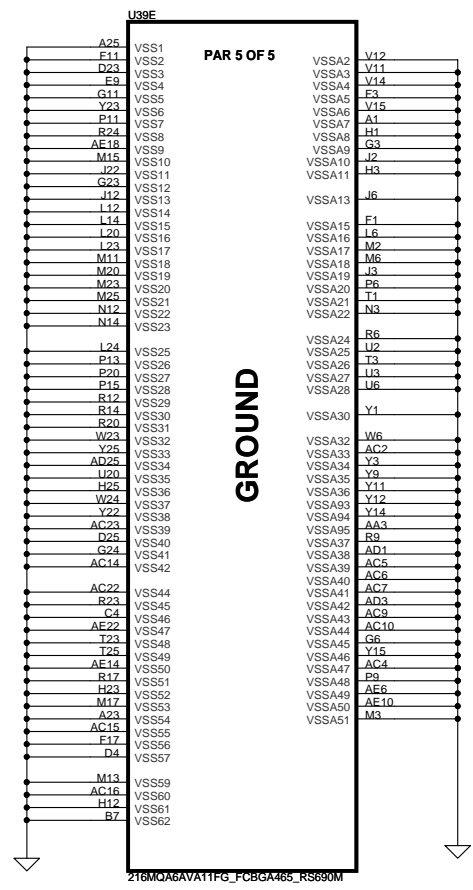
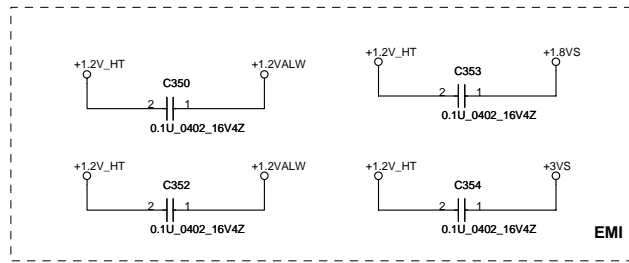
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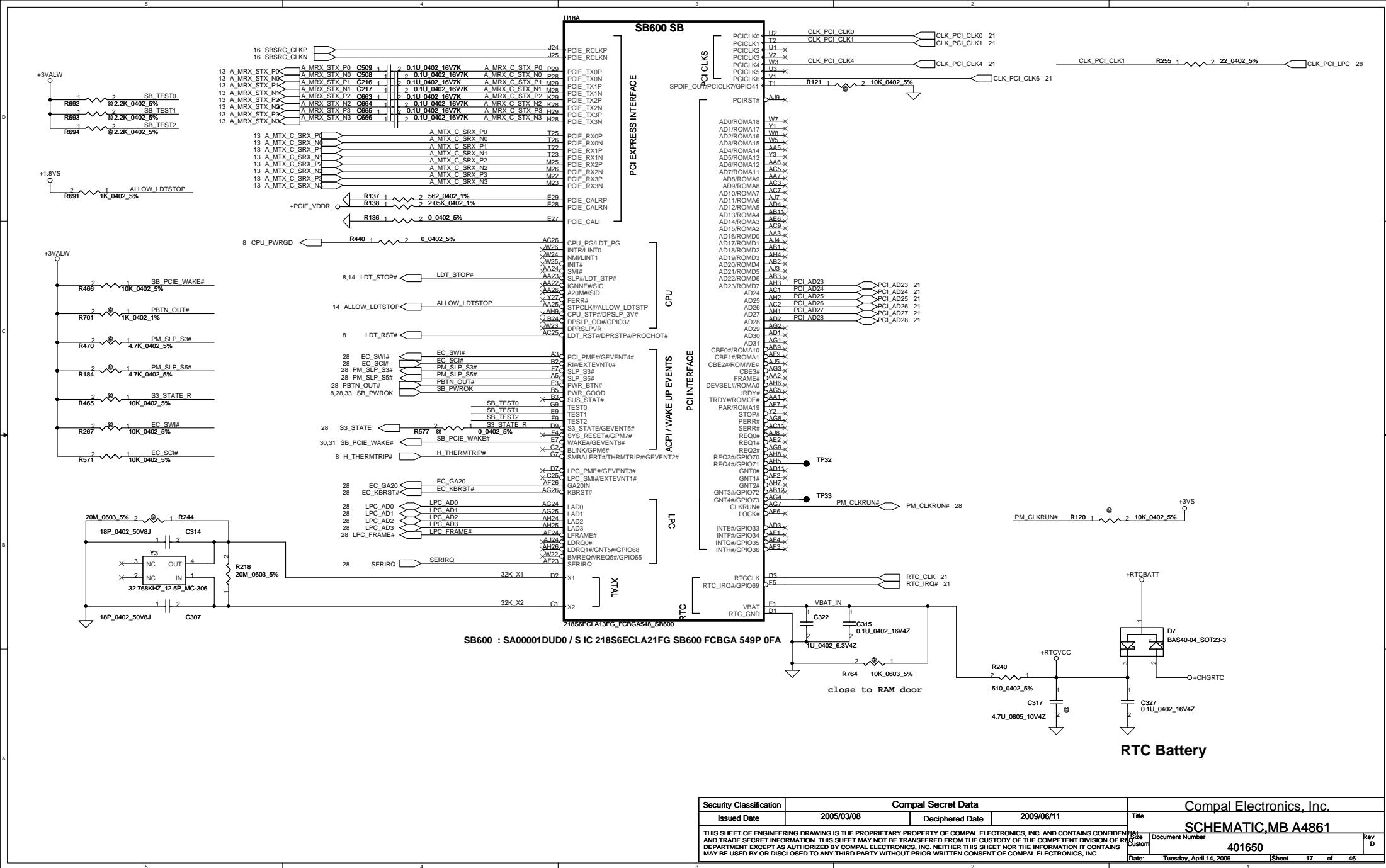


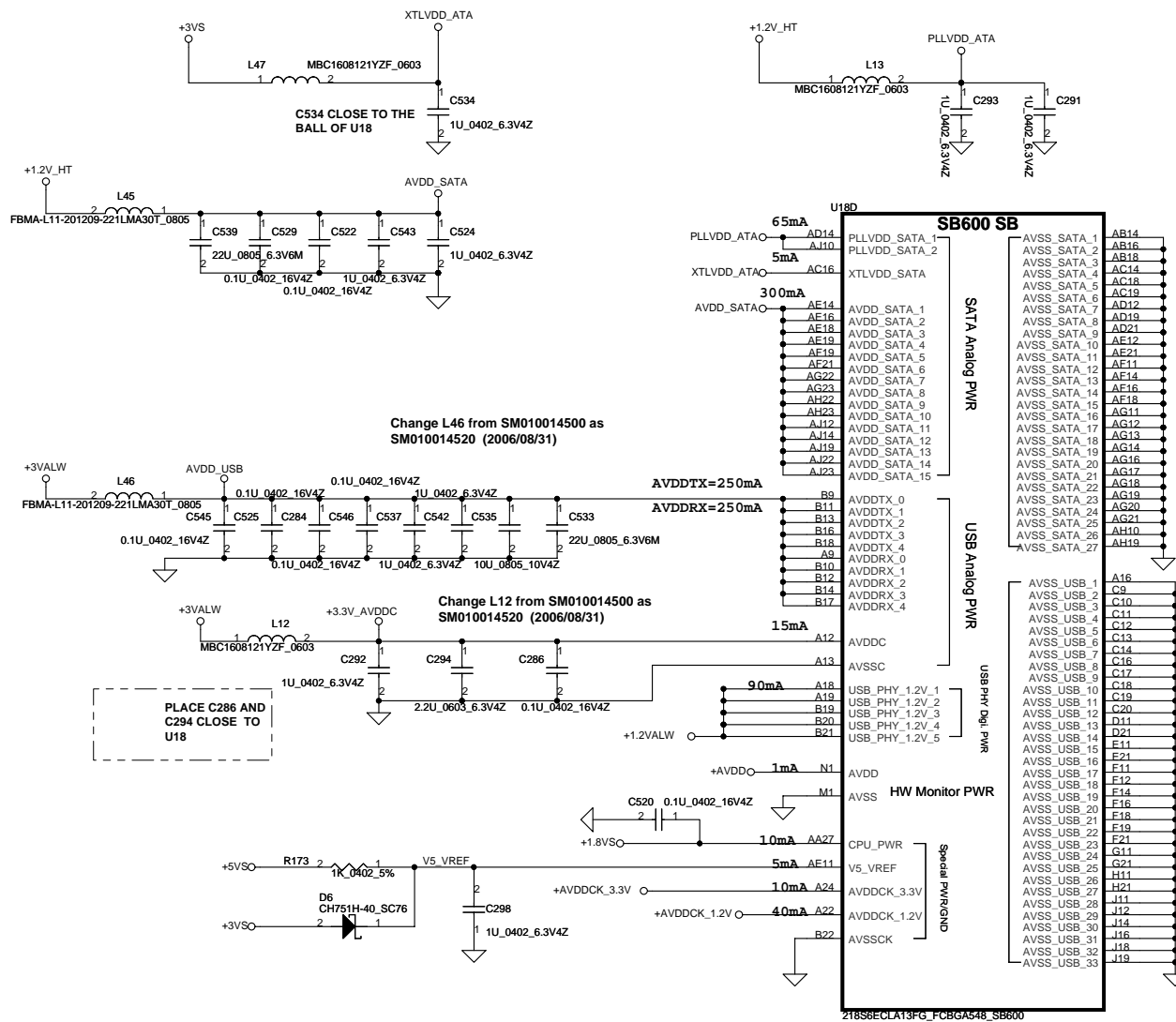
RS485: 0 Ohm RESISTOR
RS690: 220 Ohm 500mA FERRITE BEAD

RS690MC : SA00001I480 / S IC 216LQA6AVA12FG RS690MC BGA 465P 0FA



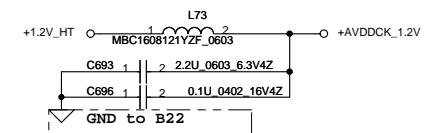
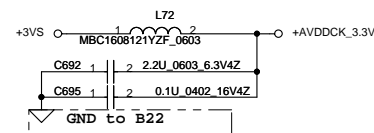
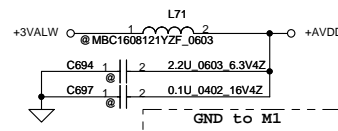
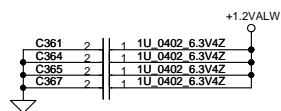
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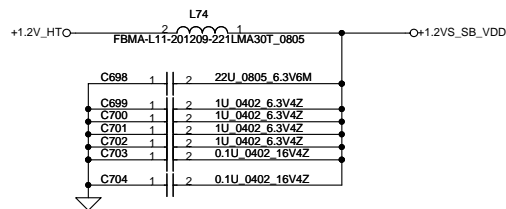
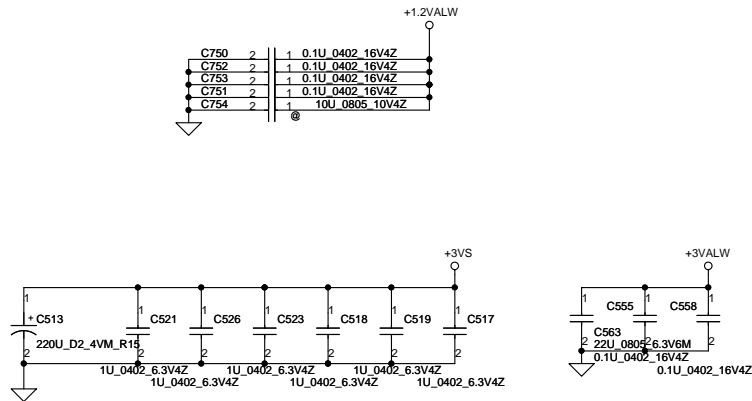


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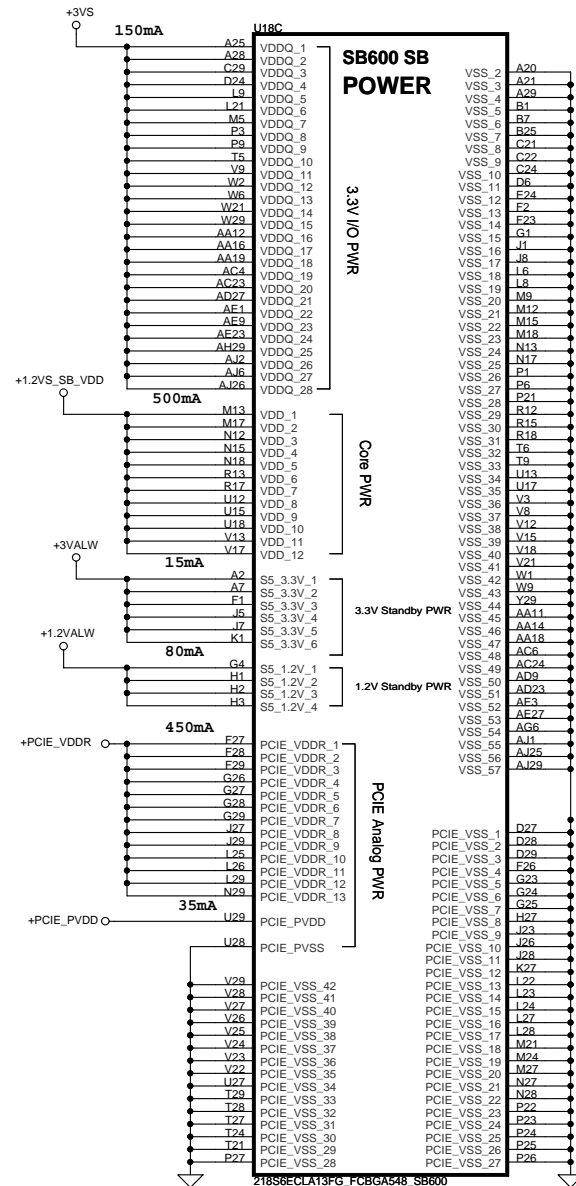
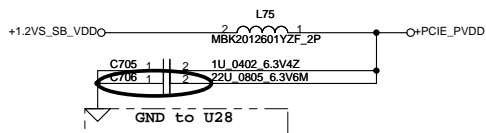
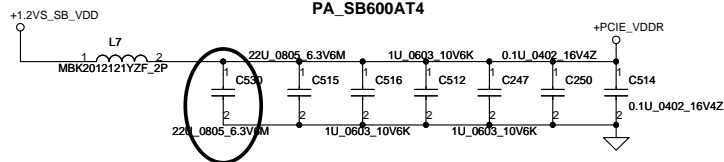
For AMD recommend change to +3.3V_S5



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Delay PCIE_VDDR / PCIE_PVDD
Add C530 to 22u
PA_SB600AT4

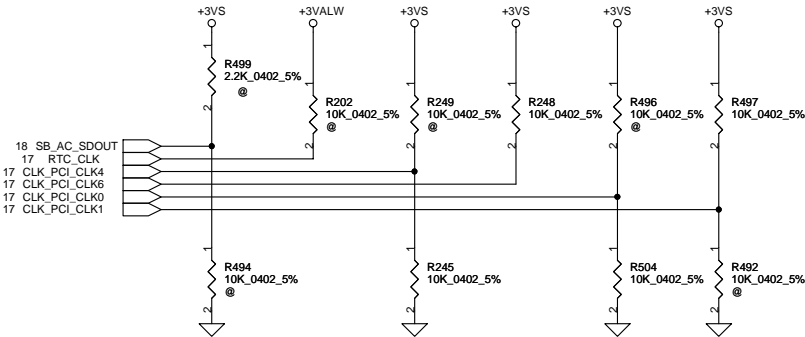


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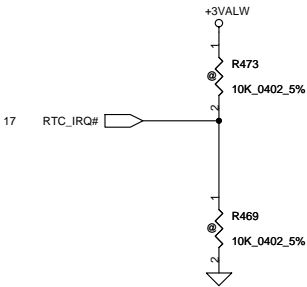
REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT,
15K PU FOR RTC_CLK, EXTERNAL PU/PD IS
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE
REQUIRED



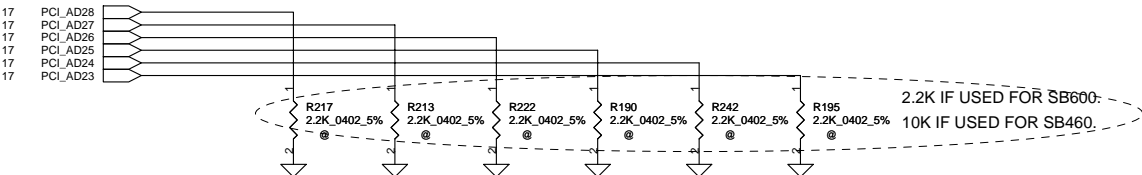
	AC_SDATA_OUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	DEFAULT	

Internal RTC: Not connected. *
External RTC: Connected to IRQ# pin on external RTC.
External RTC supports S5 wake capability (from S5 power rail or battery).



DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



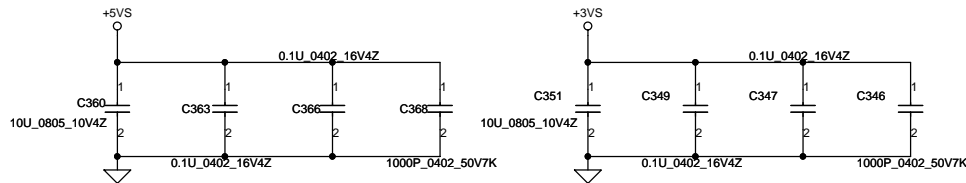
	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB600 ONLY

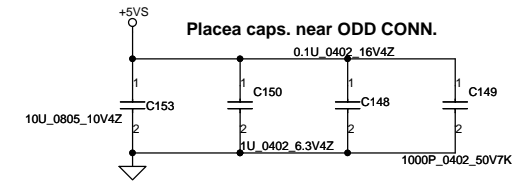
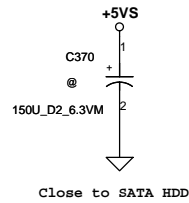
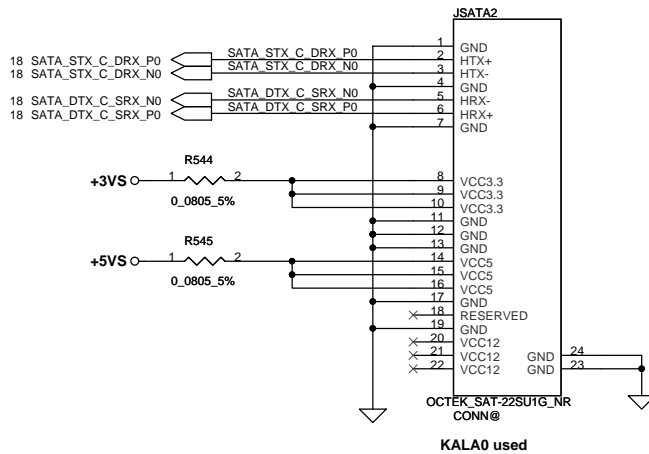
NOTE: FOR SB460, PCI_AD23 IS RESERVED

SB460 ONLY

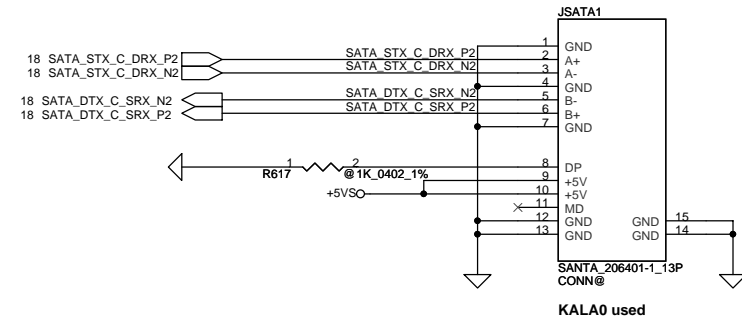
SB600 ONLY



SATA HDD CONN

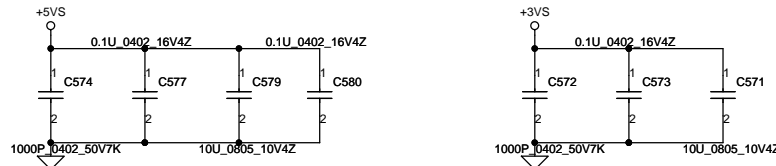
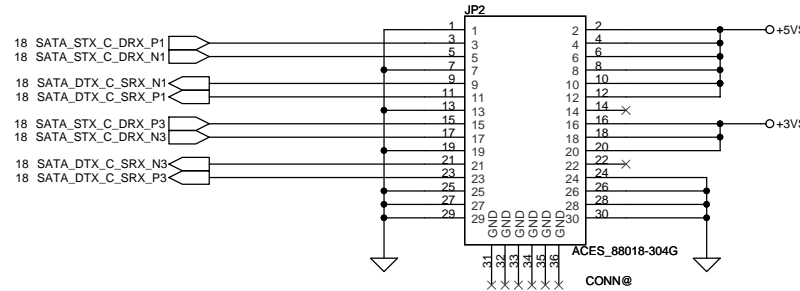


SATA ODD CONN



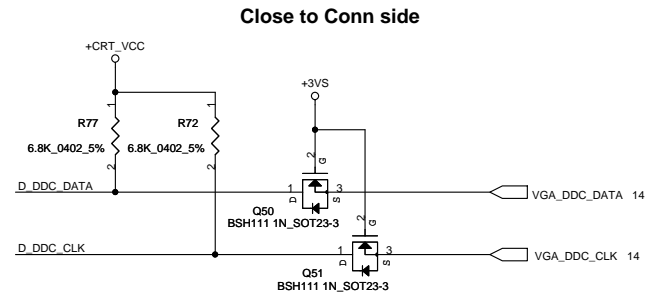
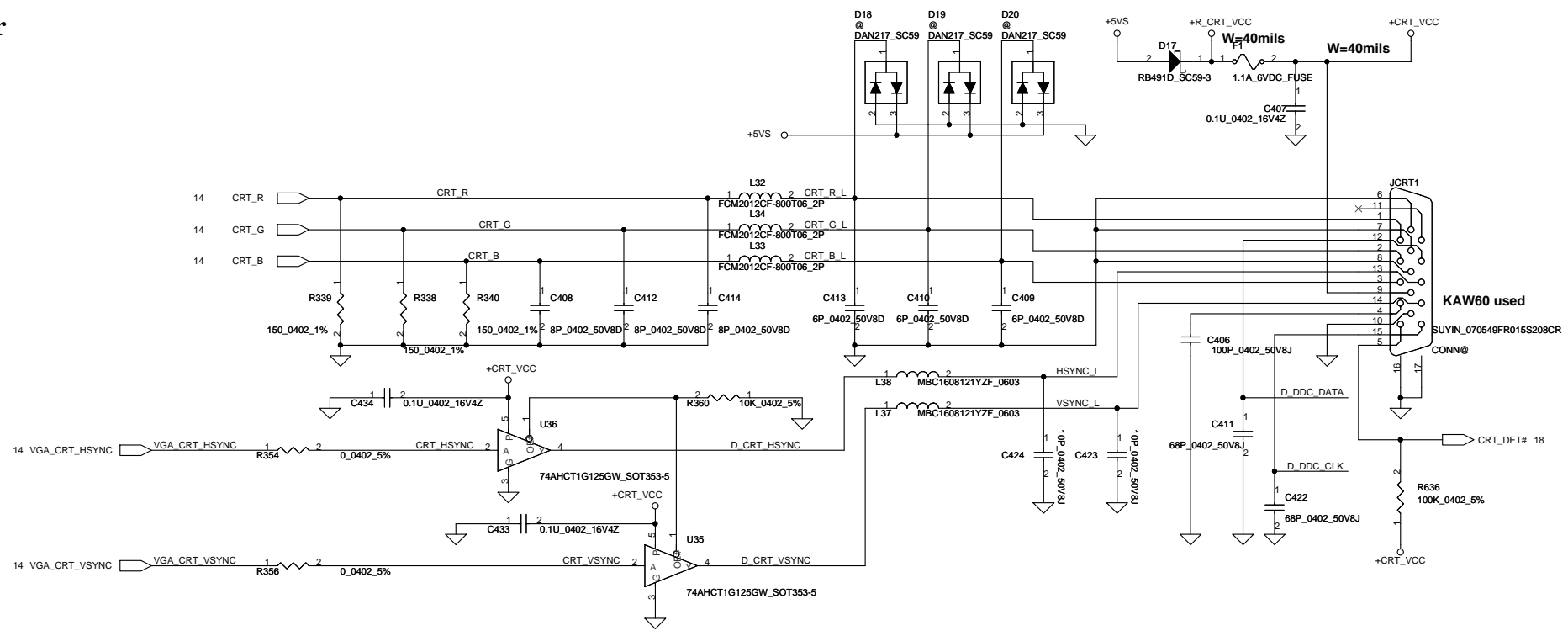
Second HDD

Second ODD



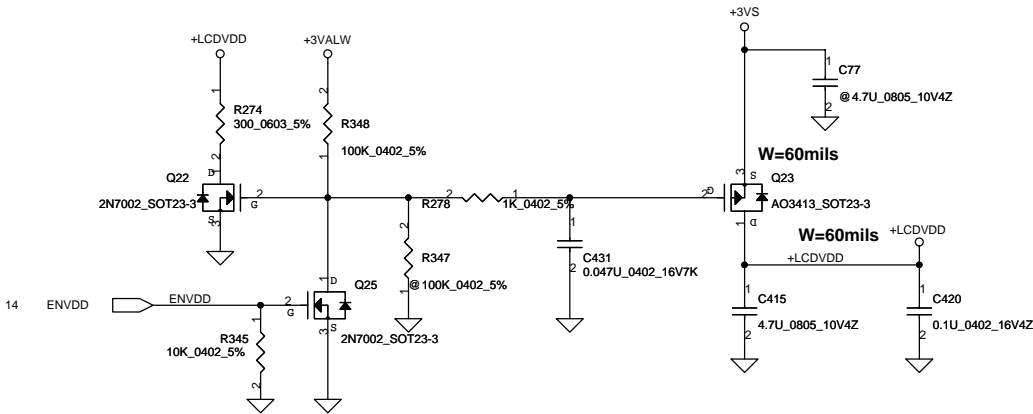
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CRT Connector

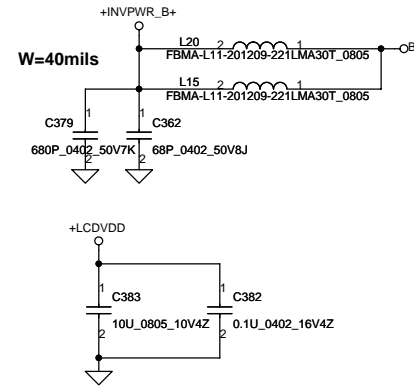
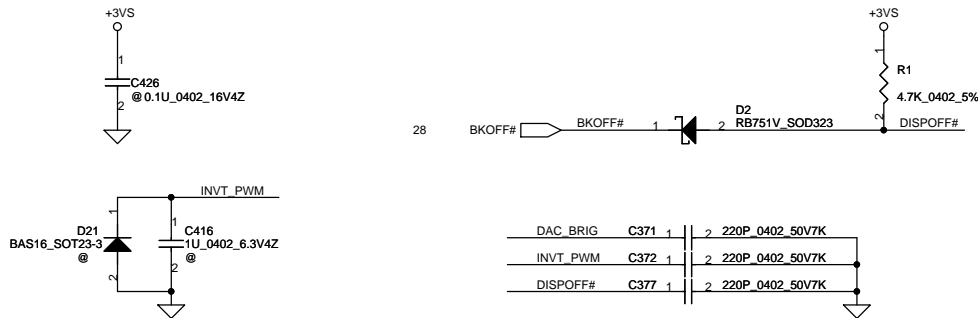
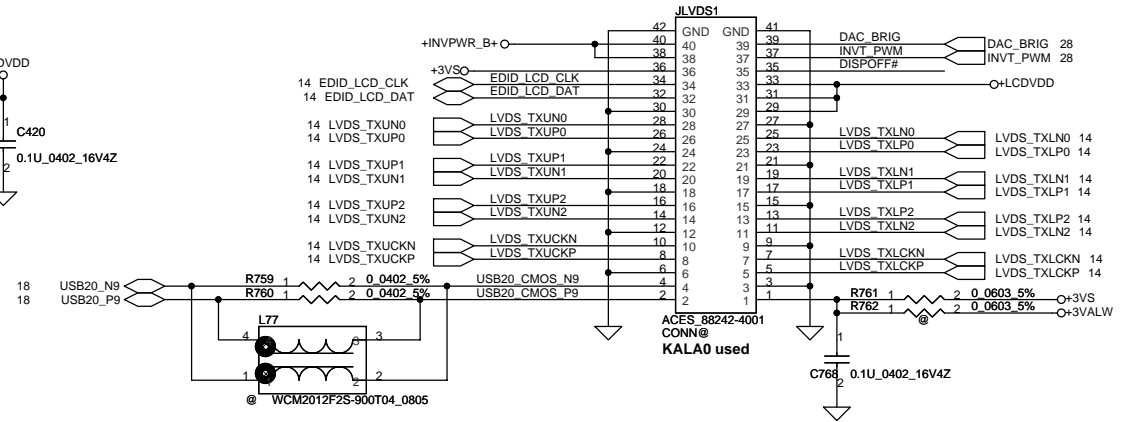


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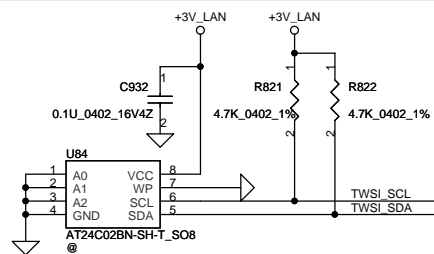
LCD POWER CIRCUIT



LCD/PANEL CONN.



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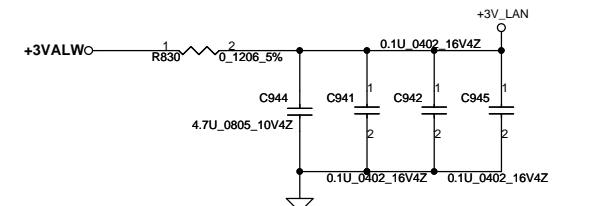


LAN MIDIO+ R843 2 1 49.9 0402 1% C978 1 2 0.1U 0402 16V4Z

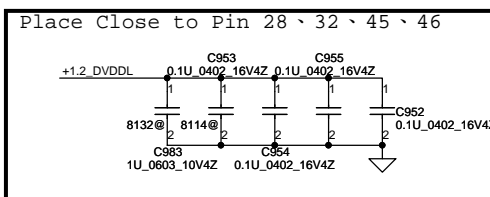
LAN MIDIO- R845 2 1 49.9 0402 1%

LAN MID1+ R846 2 1 49.9 0402 1% C979 1 2 0.1U 0402 16V4Z

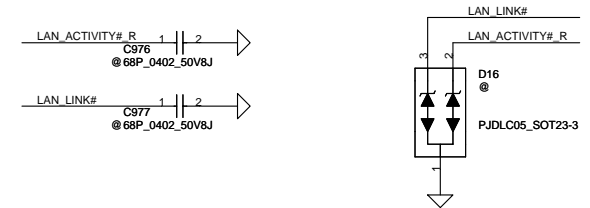
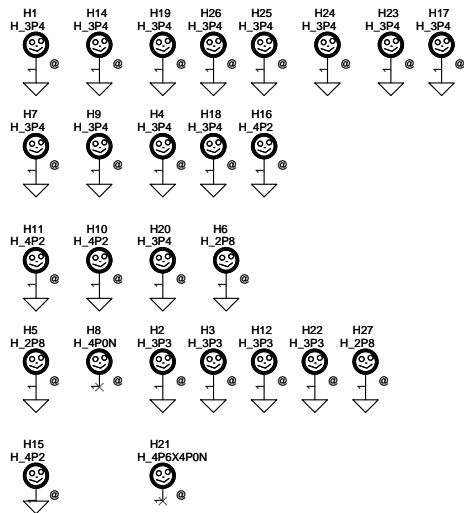
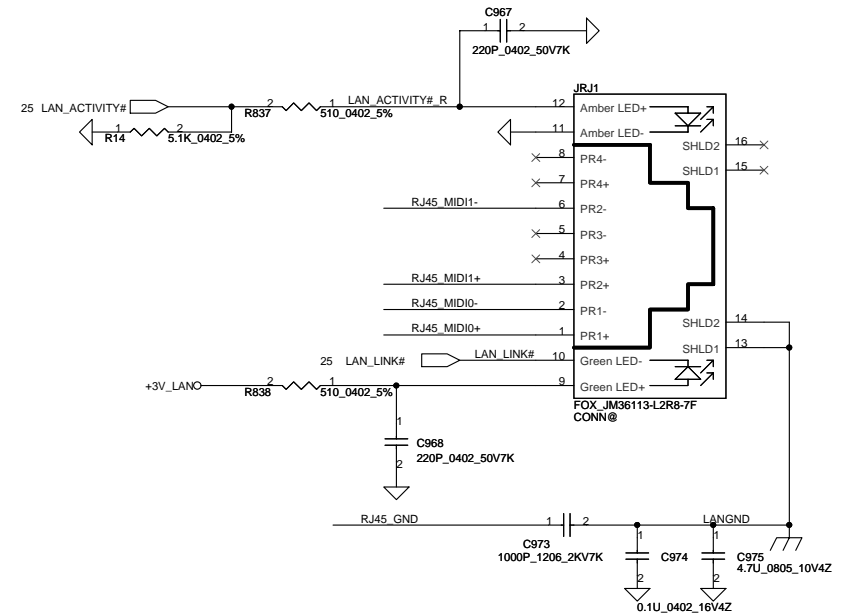
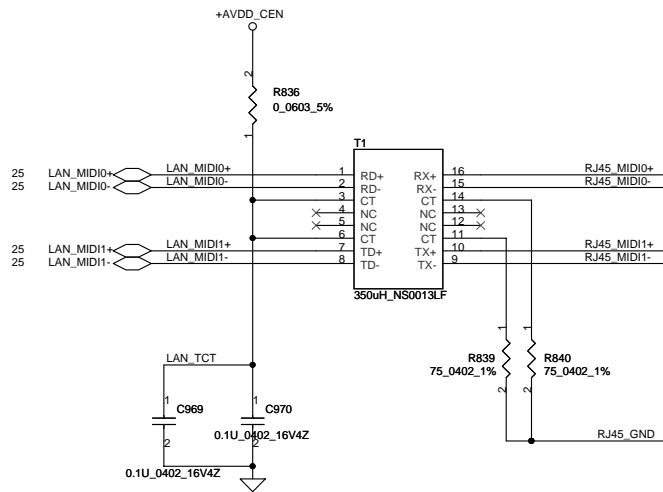
LAN MID1- R847 2 1 49.9 0402 1%



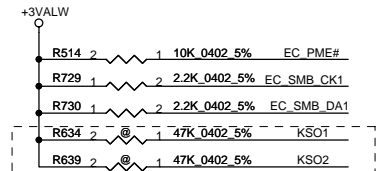
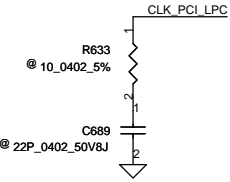
For AR8131V1



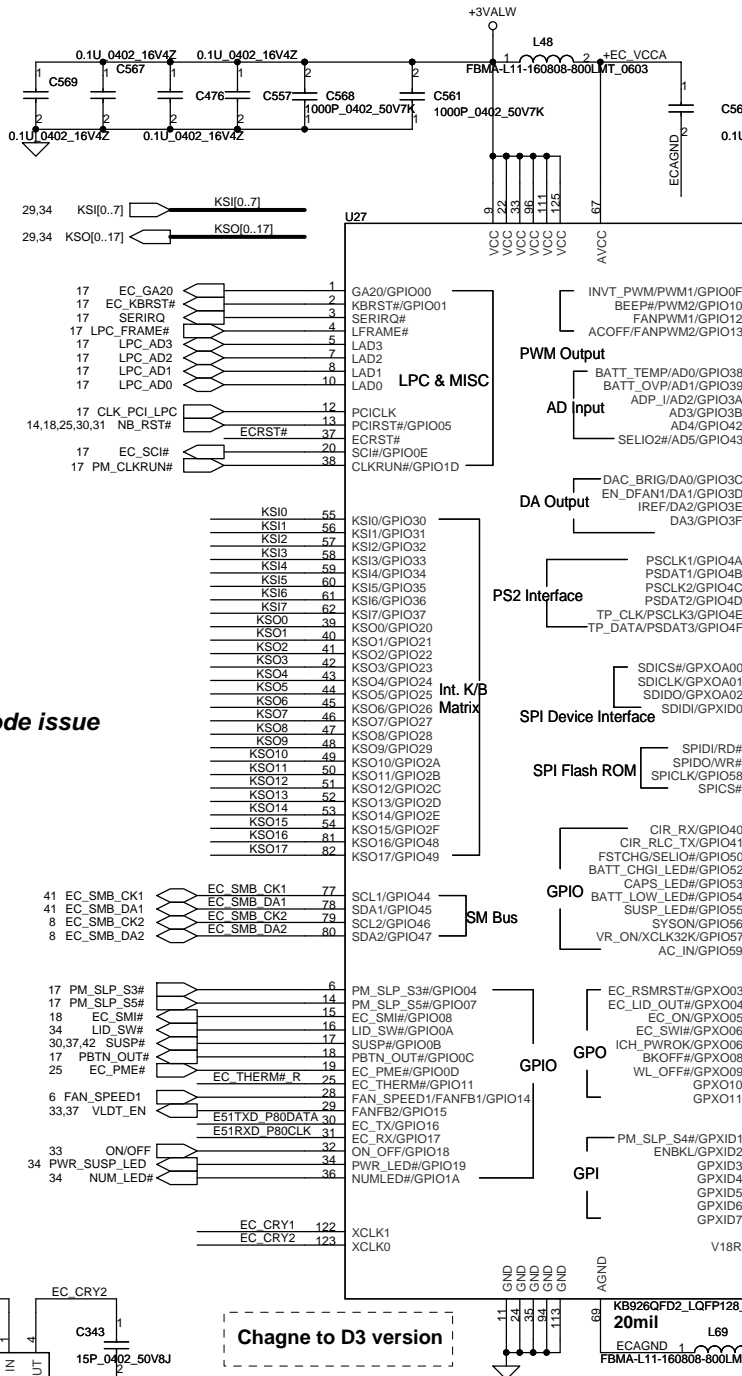
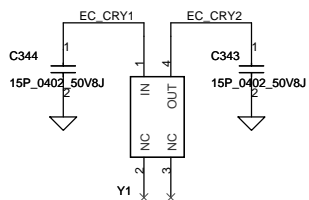
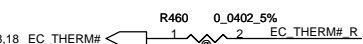
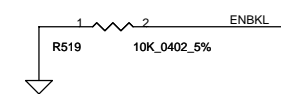
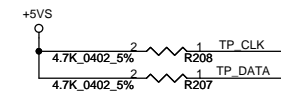
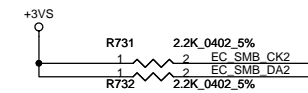
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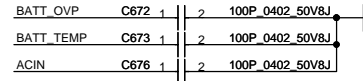


EC test-mode issue



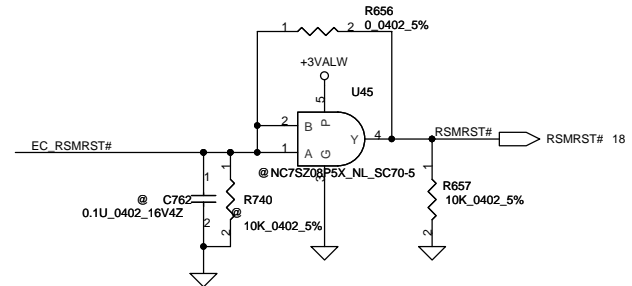
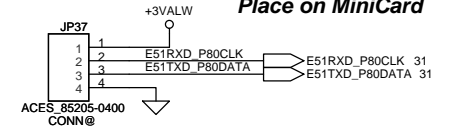
Chagne to D3 version

Please close to EC pin

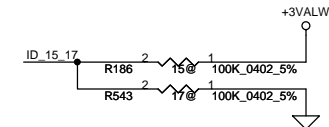


For EC Tools

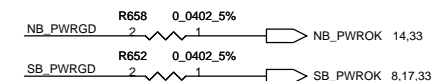
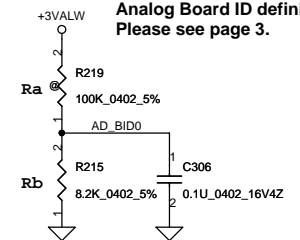
Place on MiniCard



ID DETECT
High : for 15"
Low : for 17"

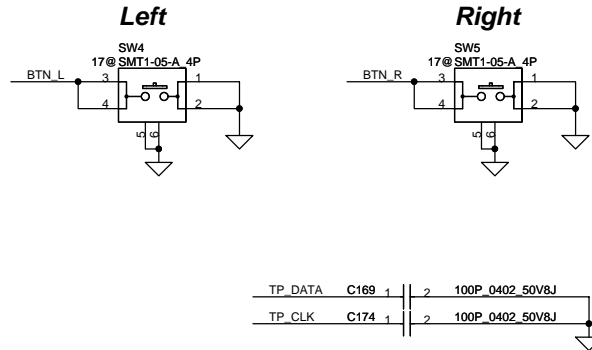


Analog Board ID definition,
Please see page 3.

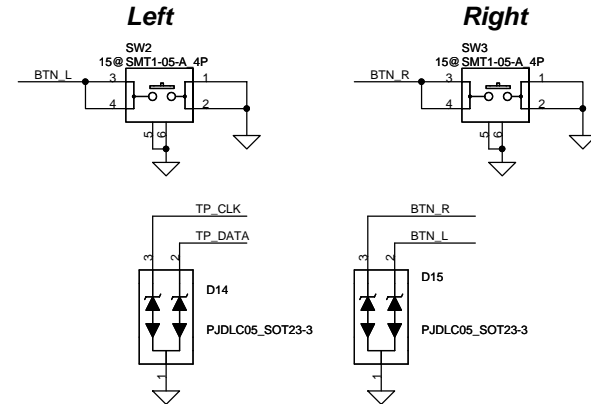


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For 17"

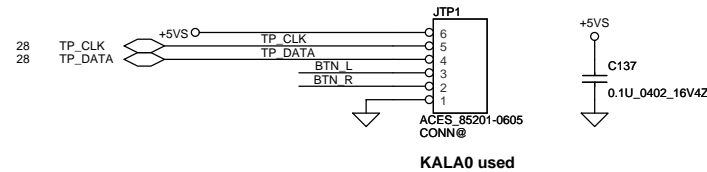


For 15"

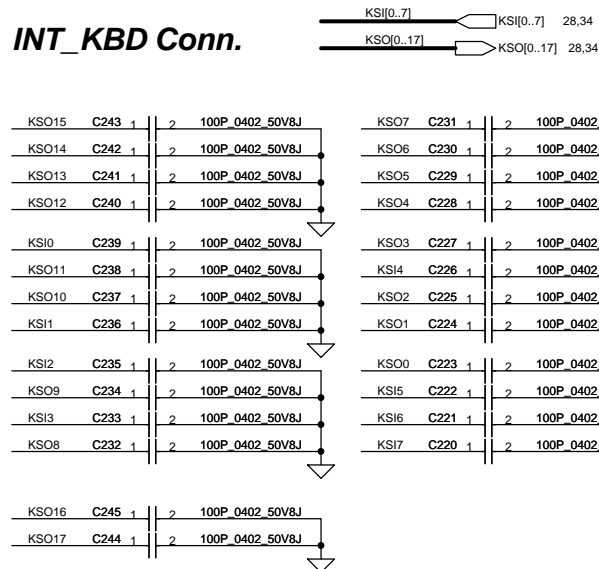


To TP/B Conn.

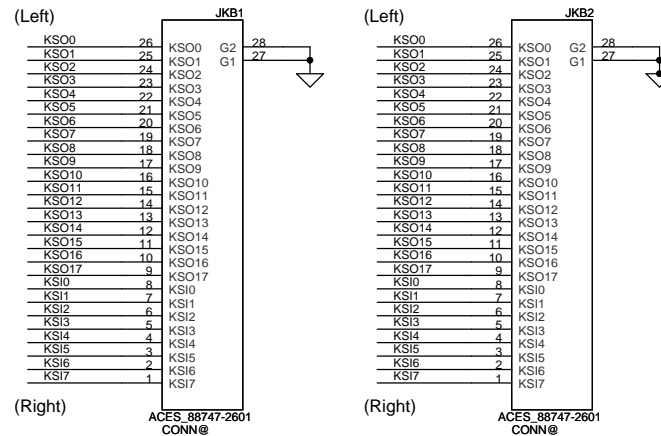
Change to SCA00000200



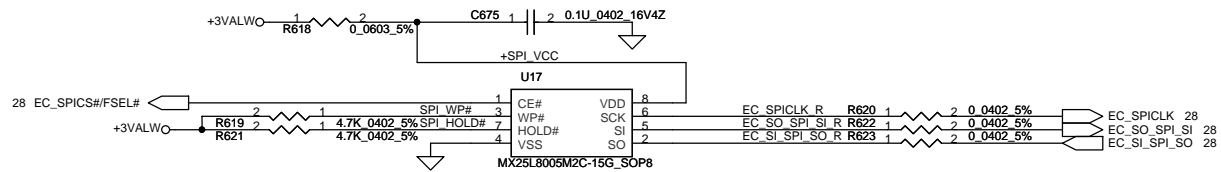
INT_KBD Conn.



KB1 for 15"
KB2 for 17"

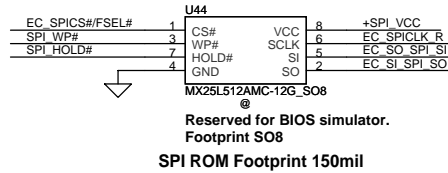
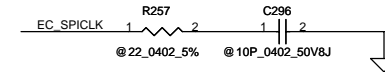


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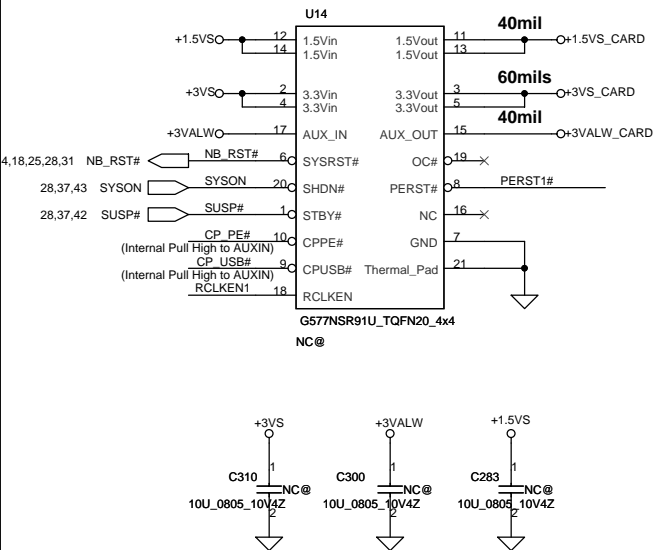


SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P
 ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

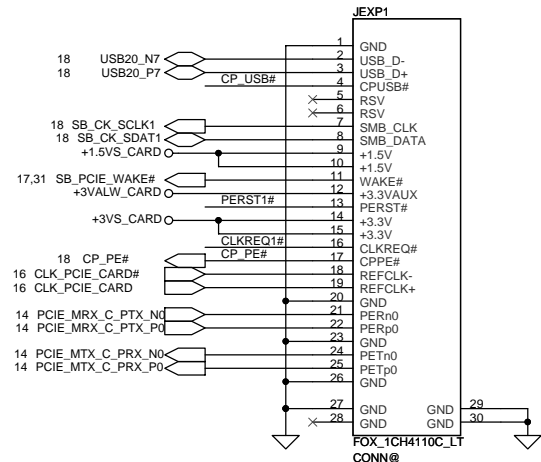
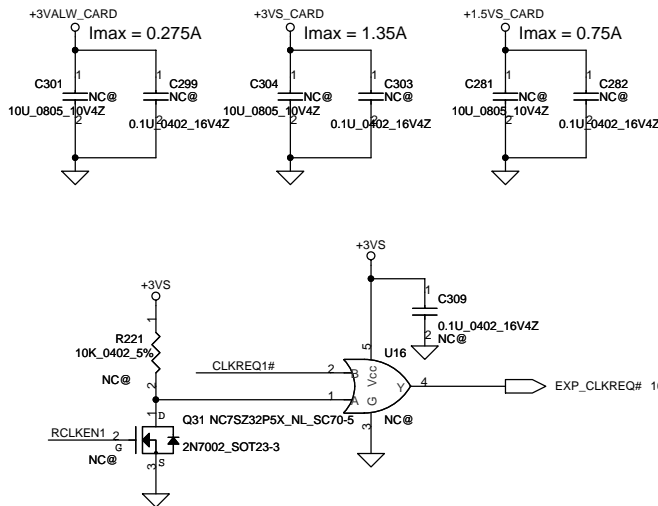
ONLY MXIC used in this project (66MHz)



New Card Power Switch

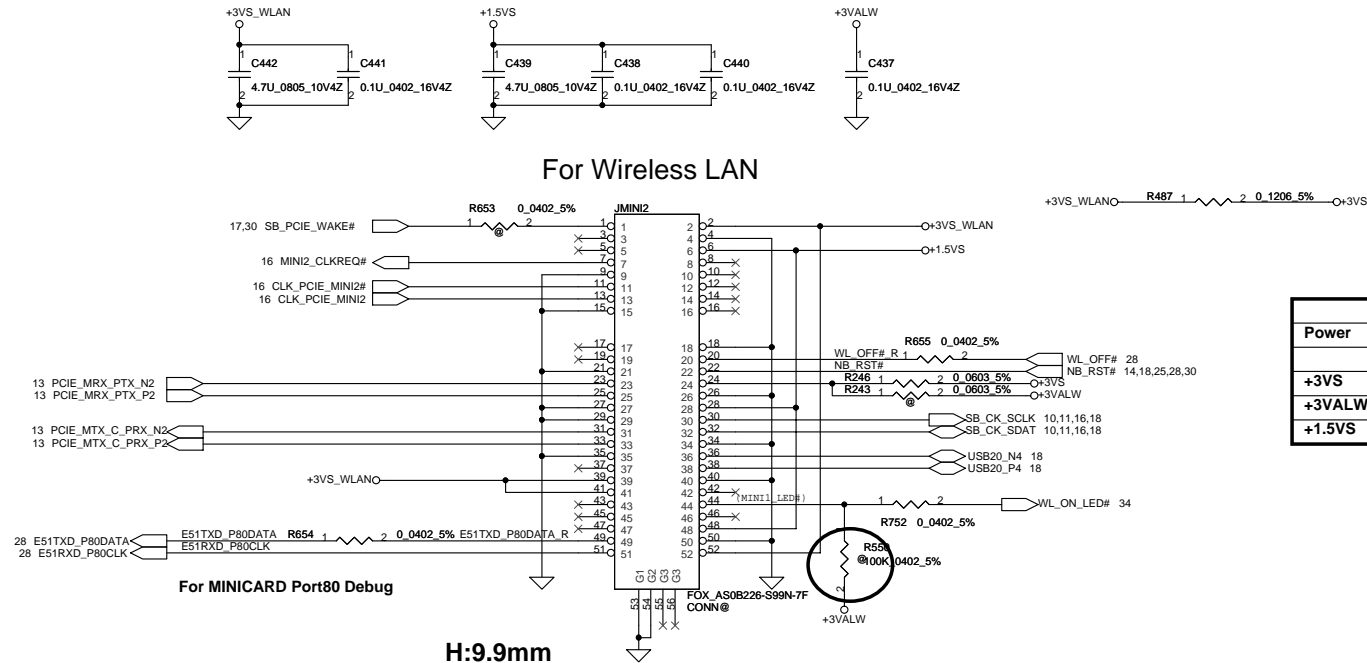


New Card Socket (Left/TOP)



Don't Connect to GND
 2008/02/22

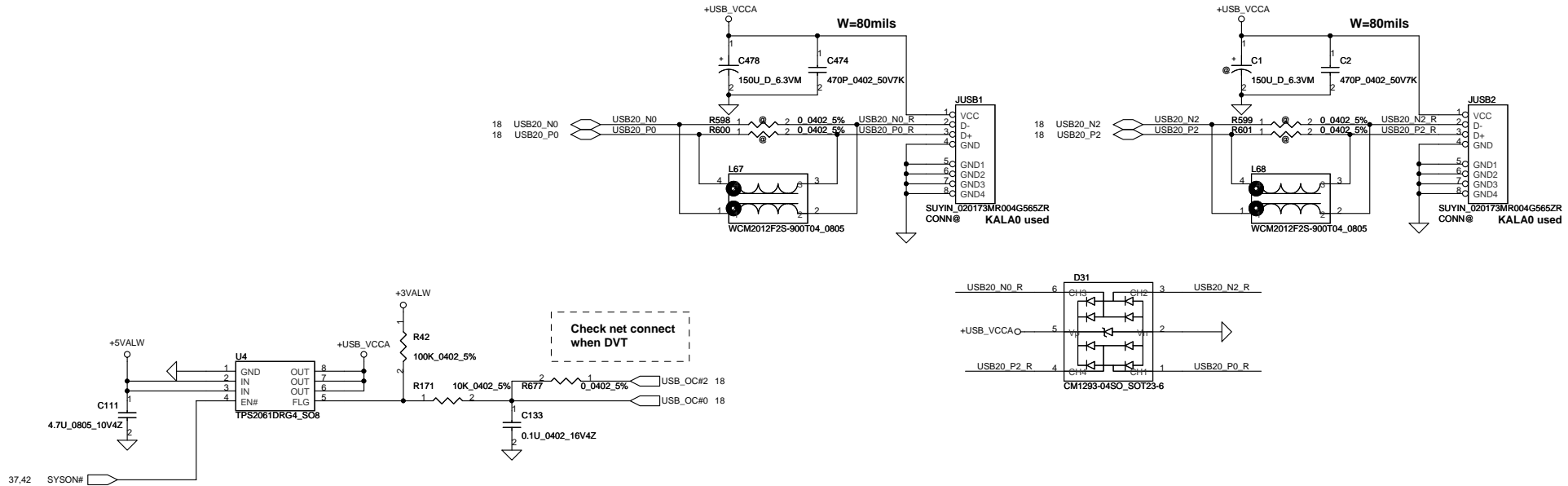
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Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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USB CONN. 1 & 2



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								Rev A		Document Number		401650		Rev D	
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Power ON Circuit

The schematic shows the power-on sequence for the system. It begins with the VLDT_EN input (pins 28,37) which is pulled up by R106 (10K_0402_5%) and passes through R100 (47K_0402_1%) to a Schmitt trigger inverter U10A (SN74LVC14APWR_TSSOP14). The output of U10A is connected to a +3V power supply and a network of resistors (R111, R112, R109, R113) and capacitors (C203, C204). This network drives a series of inverters U10E, U10F, U10D, and U10C. The final output is connected to SB_PWROK (pins 8,17,28) and NB_PWROK (pins 14,28) through resistors R104, R105, R108, and R110. The circuit is powered by +3V and +3VALW supplies.

Timing diagram showing the relationship between VLDLT_EN, NB_PWRGD, SB_PWRGD, SUSP#, and +1.8VS. The diagram includes two time intervals, T1 and T2, marked by vertical dashed lines. VLDLT_EN is high during T1. NB_PWRGD and SB_PWRGD are high during T2. SUSP# is high during T2. +1.8VS is high throughout the duration shown.

Power Button

TOP SIDE

Bottom Side

34 ON/OFFBTN#

ON/OFFBTN#

1

2

1

R765 10K_0603_5%

R766 10K_0603_5%

D10 DAN202UT106_SC70-3

2

3

51ON#

ON/OFF

28

51ON#

38

+3V3LW

R281 100K_0402_5%

2

1

C358 1000P_0402_50V7K

D11 RLZ20A_LL34

Q17 2N7002_SOT23

R290 10K_0402_5%

2

1

3

EC_ON

28

SW10 SMT1-05-A_4P

1

2

3

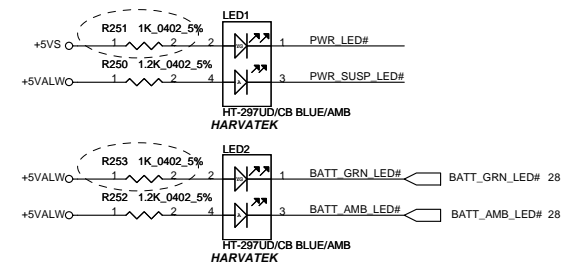
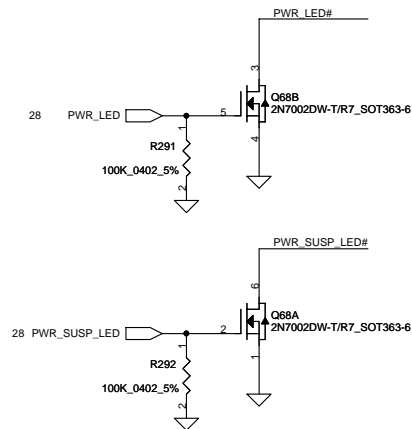
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ON/OFFBTN#

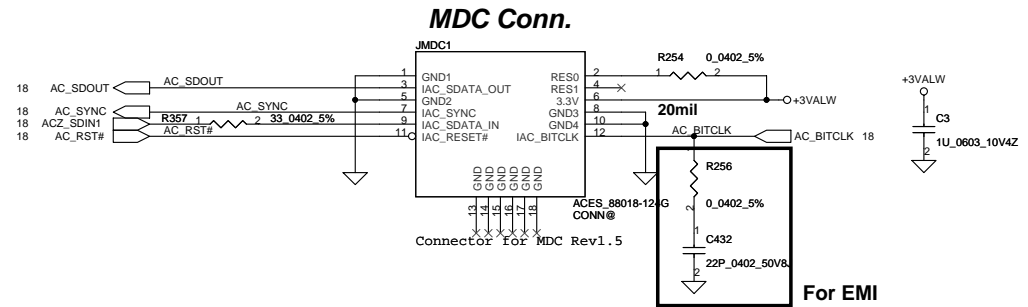
MP would remove

MP would remove

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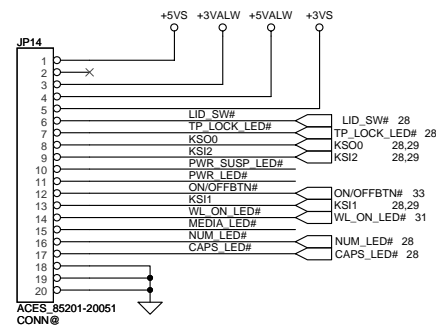


BLUE/AMB LED

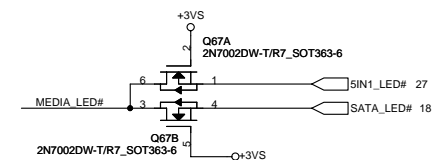
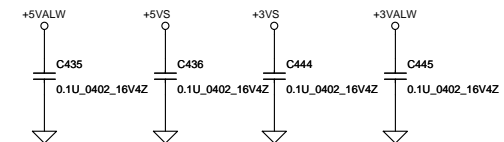


For EMI

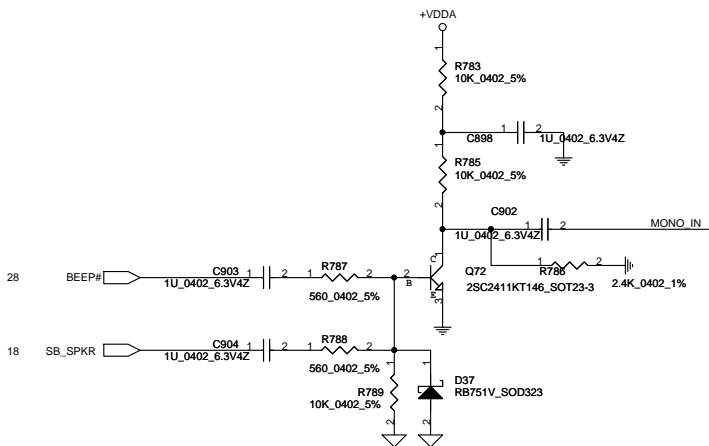
To PWR LED/B



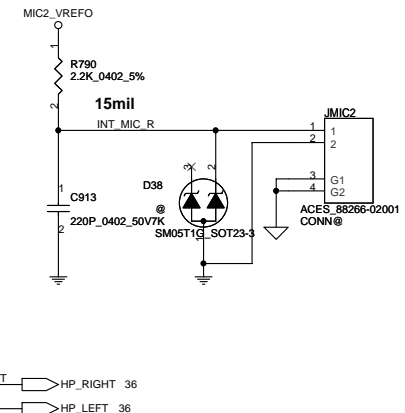
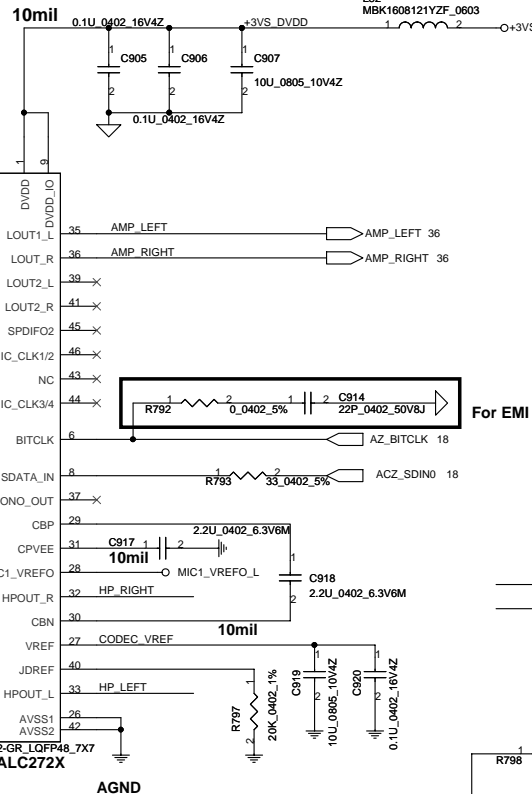
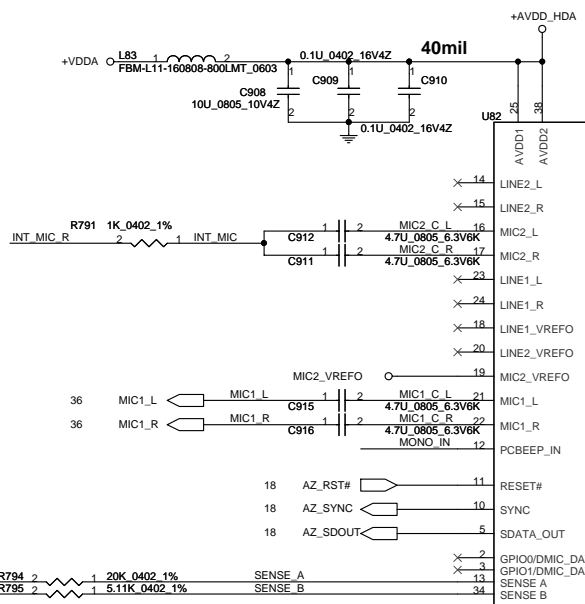
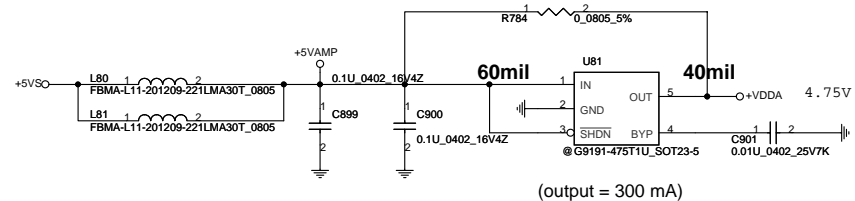
	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	



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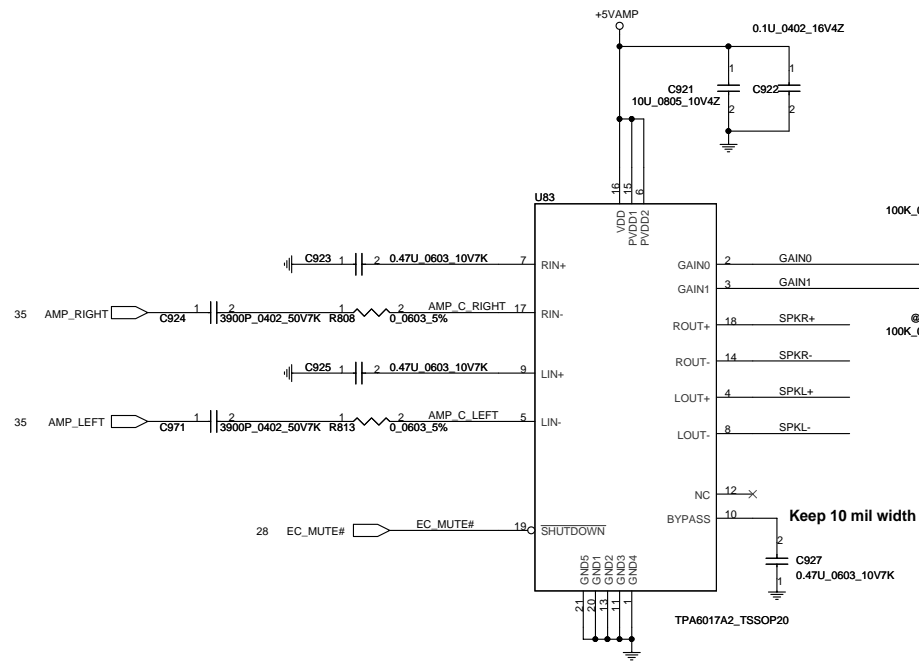
HD Audio Codec



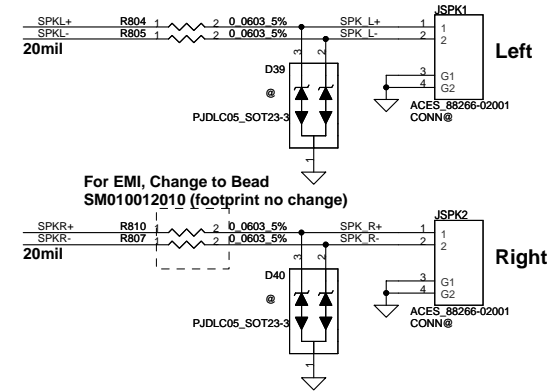
update this table

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

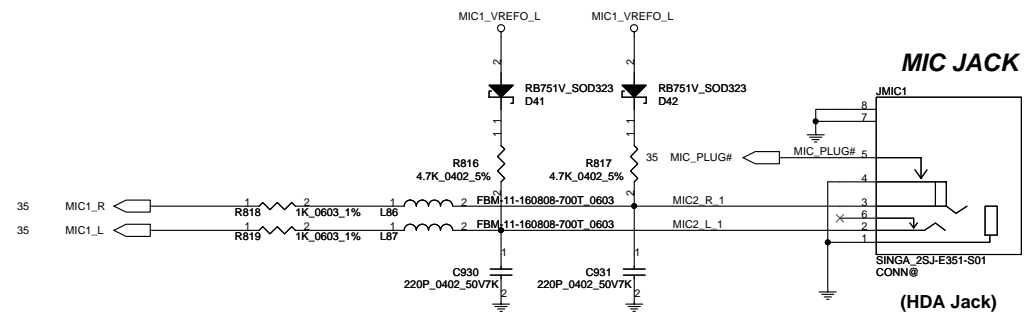
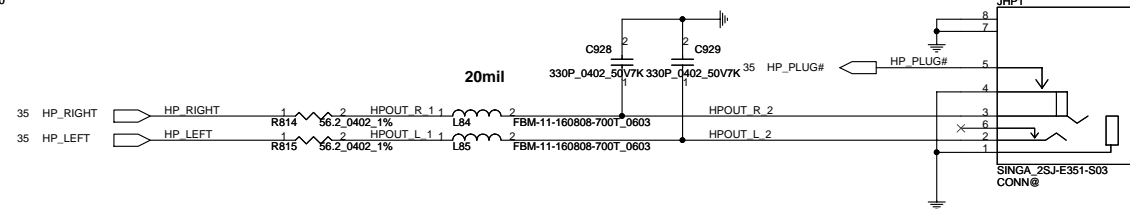
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2007/09/20				2009/06/11				Title			
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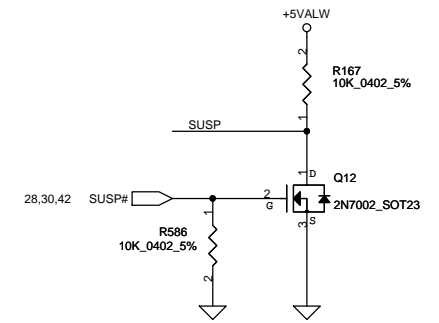
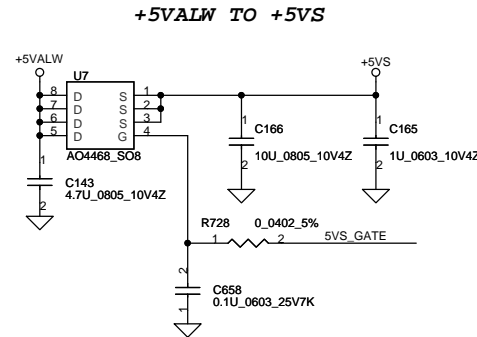
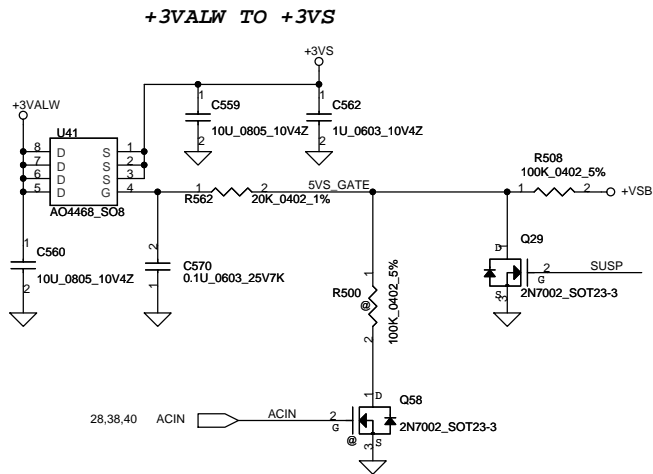
Int. Speaker Conn.



LINE Out/Headphone Out

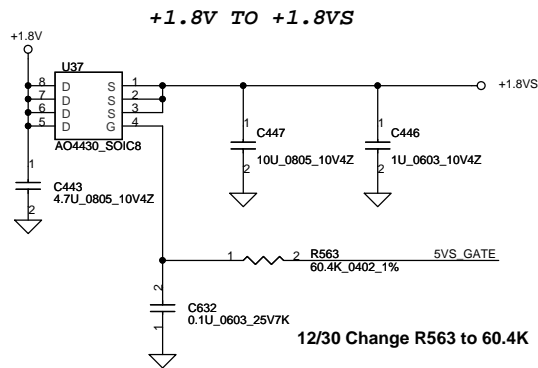
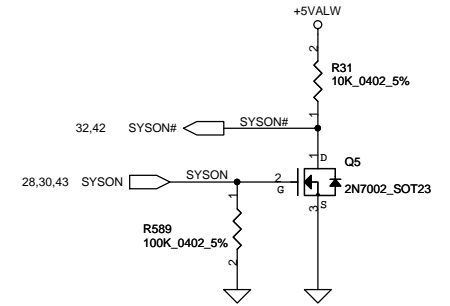
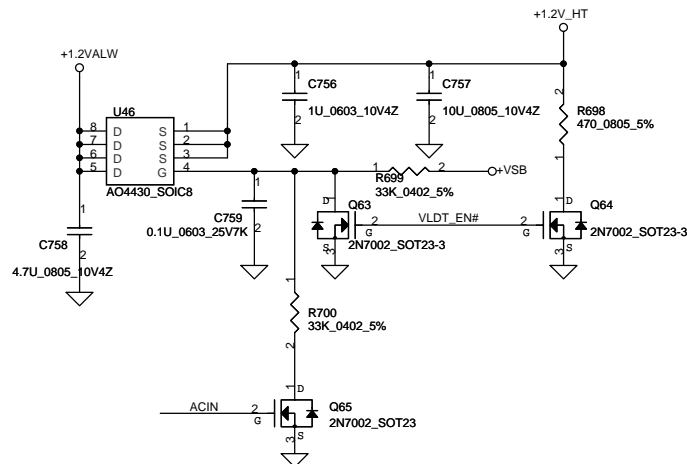


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										401650			
										Date		Friday, April 10, 2009	

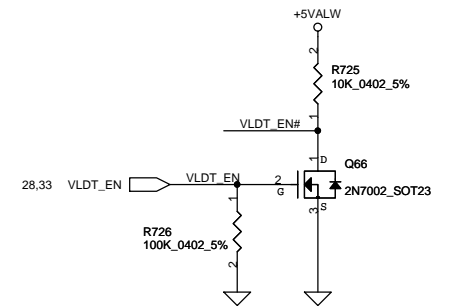


2006/2/22 Add C658 0.1uF

+1.2VALW TO +1.2V_HT

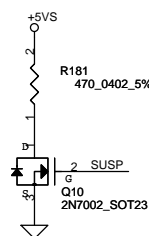
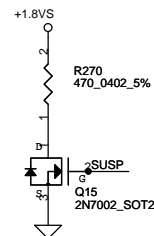
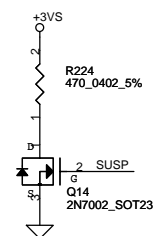
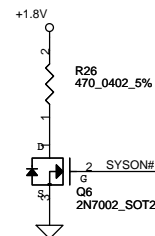
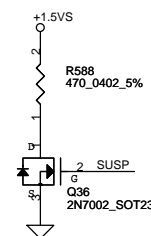
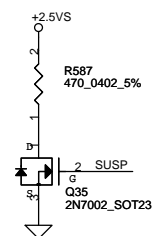
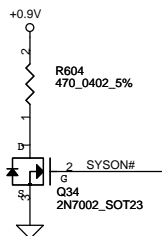


12/30 Change R563 to 60.4K

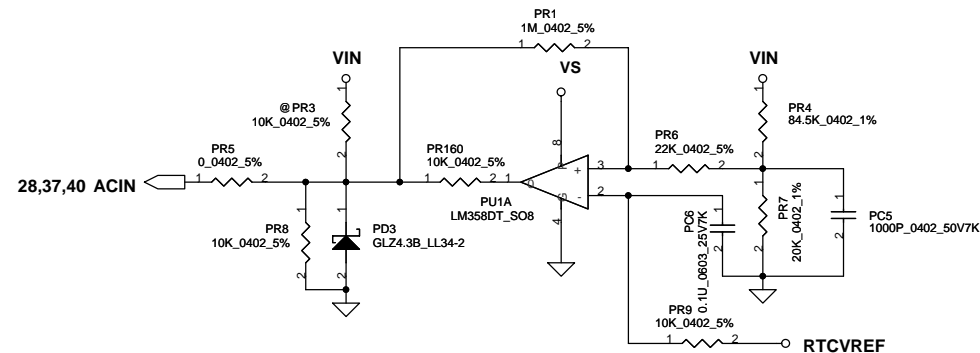
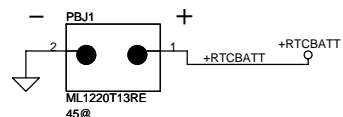


Near PU8

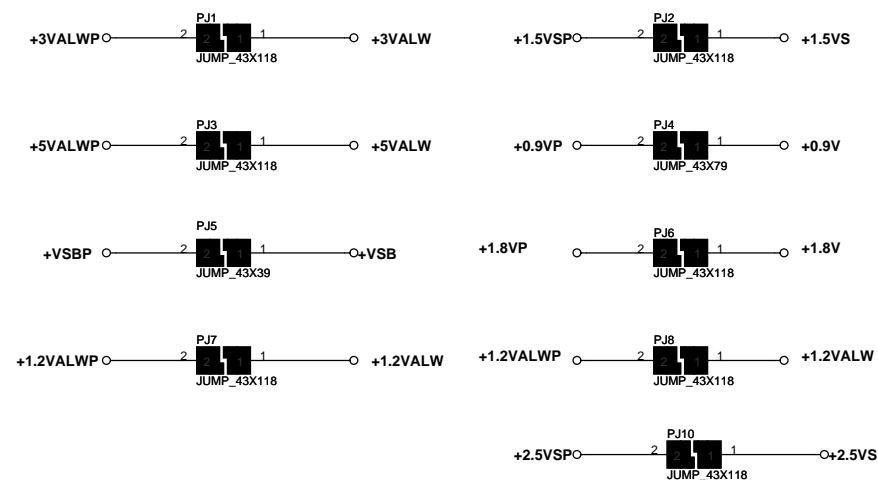
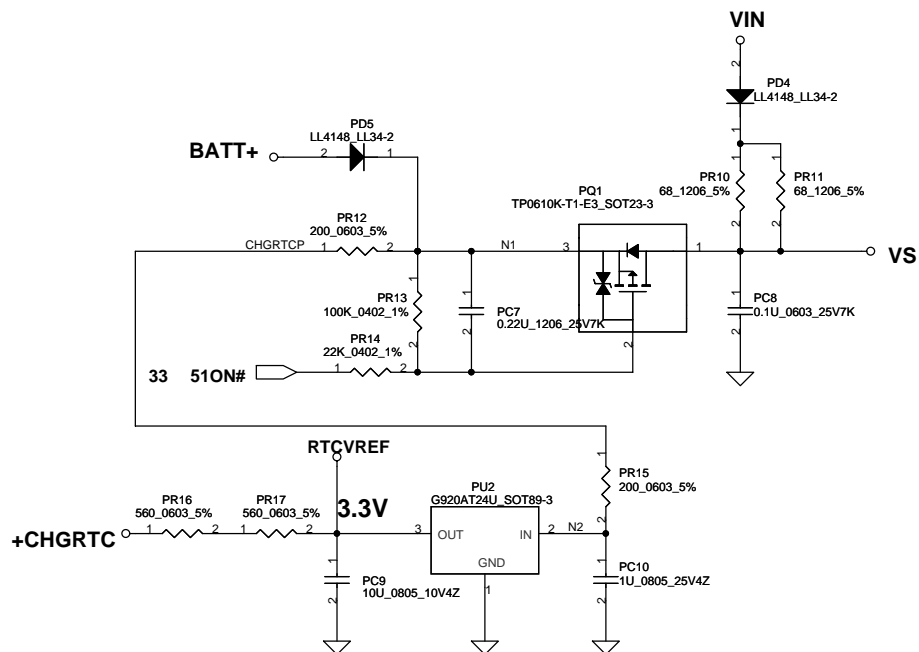
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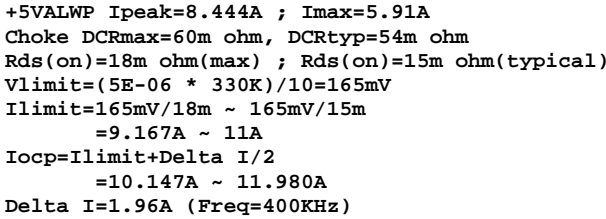


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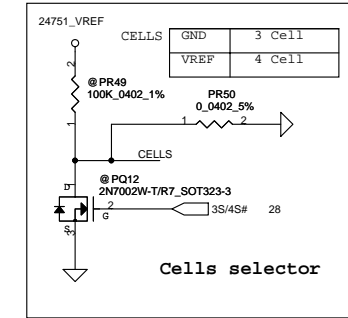
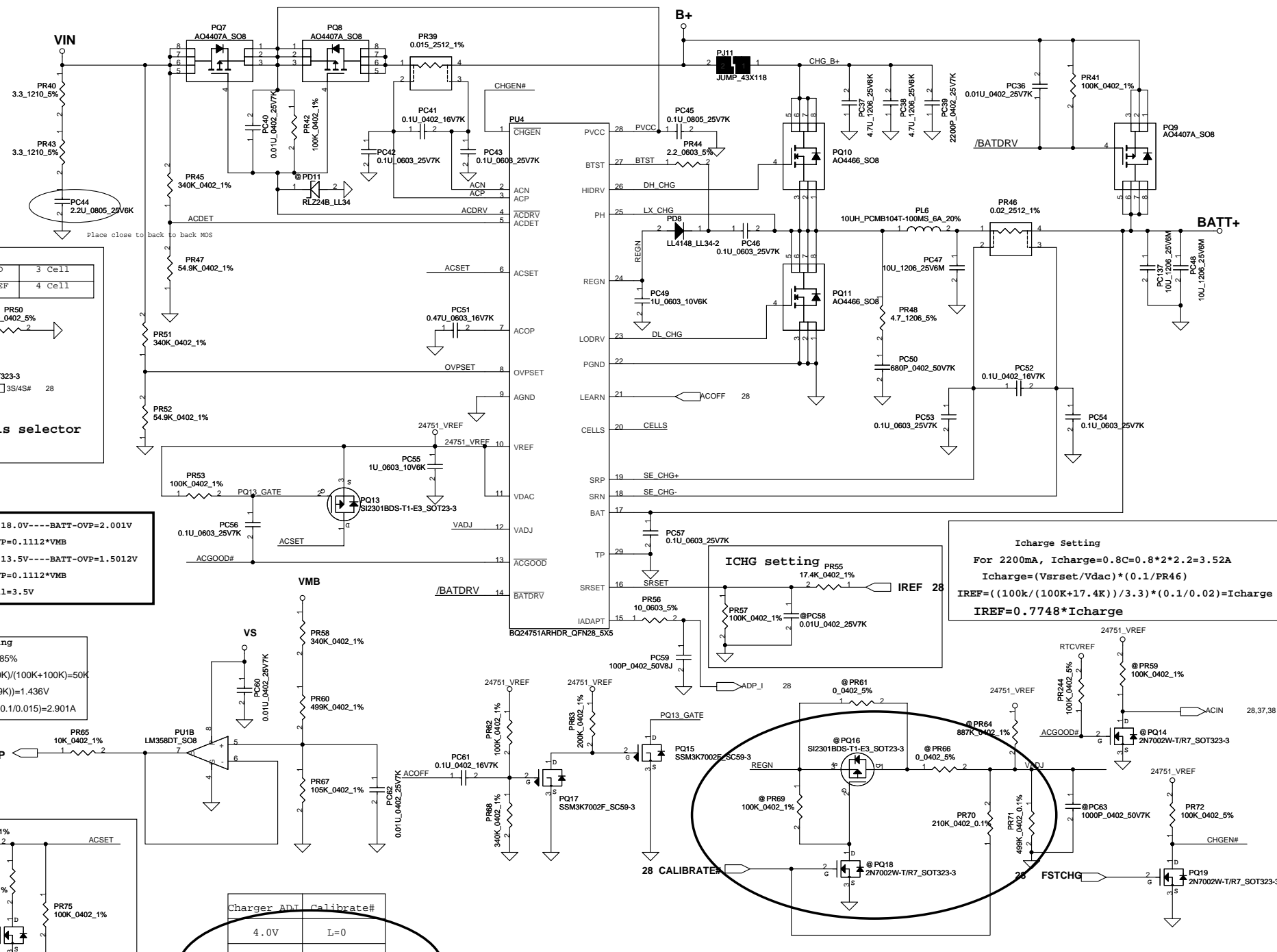


Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V





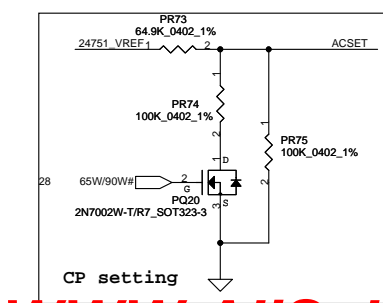
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Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz

LI-4S : 18.0V----BATT-OVP=2.001V
 BATT-OVP=0.1112*VMB
 LI-3S : 13.5V----BATT-OVP=1.5012V
 BATT-OVP=0.1112*VMB
 Per cell=3.5V

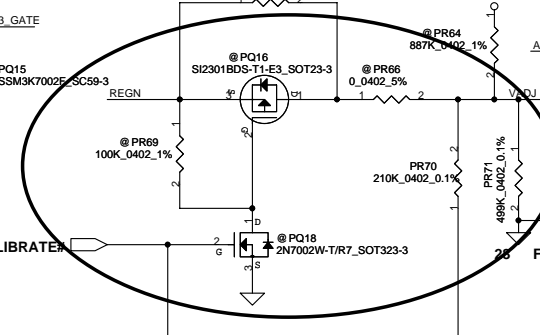
CP Point Setting
 CP point=ladapter*85%
 65W adapter R=(100K*100K)/(100K+100K)=50K
 Vacset=3.3*(50K/(50K+64.9K))=1.436V
 CP POINT=(1.436V/3.3V)*(0.1/0.015)=2.901A



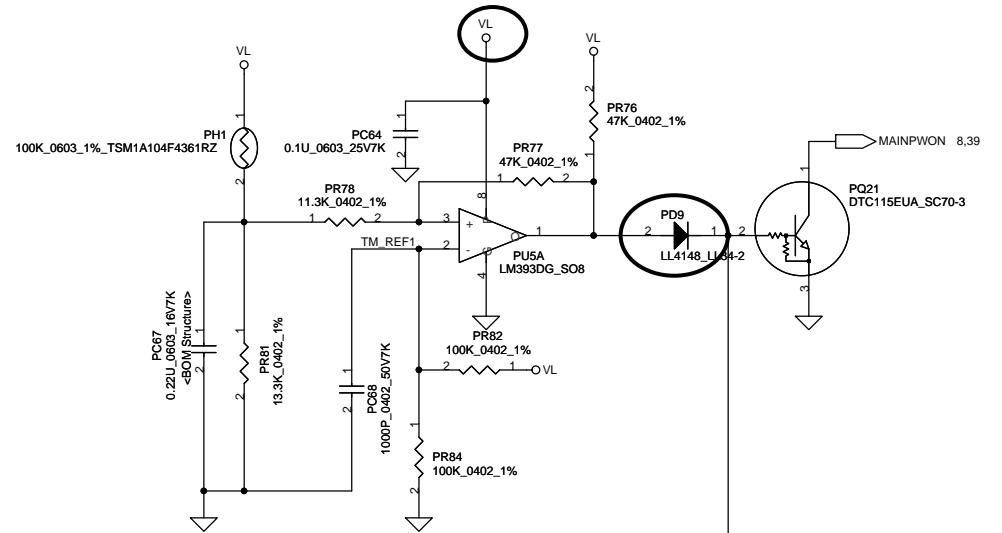
Charger ADI	Calibrate#
4.0V	L=0
4.2V	1.8755V
4.3V	2.8132V
4.35V	H=3.3V

ICHG setting
 For 2200mA, Icharge=0.8C=0.8*2*2.2=3.52A
 Icharge=(Vsrset/Vdac)*(0.1/PR46)
 IREF=((100k/(100K+17.4K))/3.3)*(0.1/0.02)=Icharge
 IREF=0.7748*Icharge

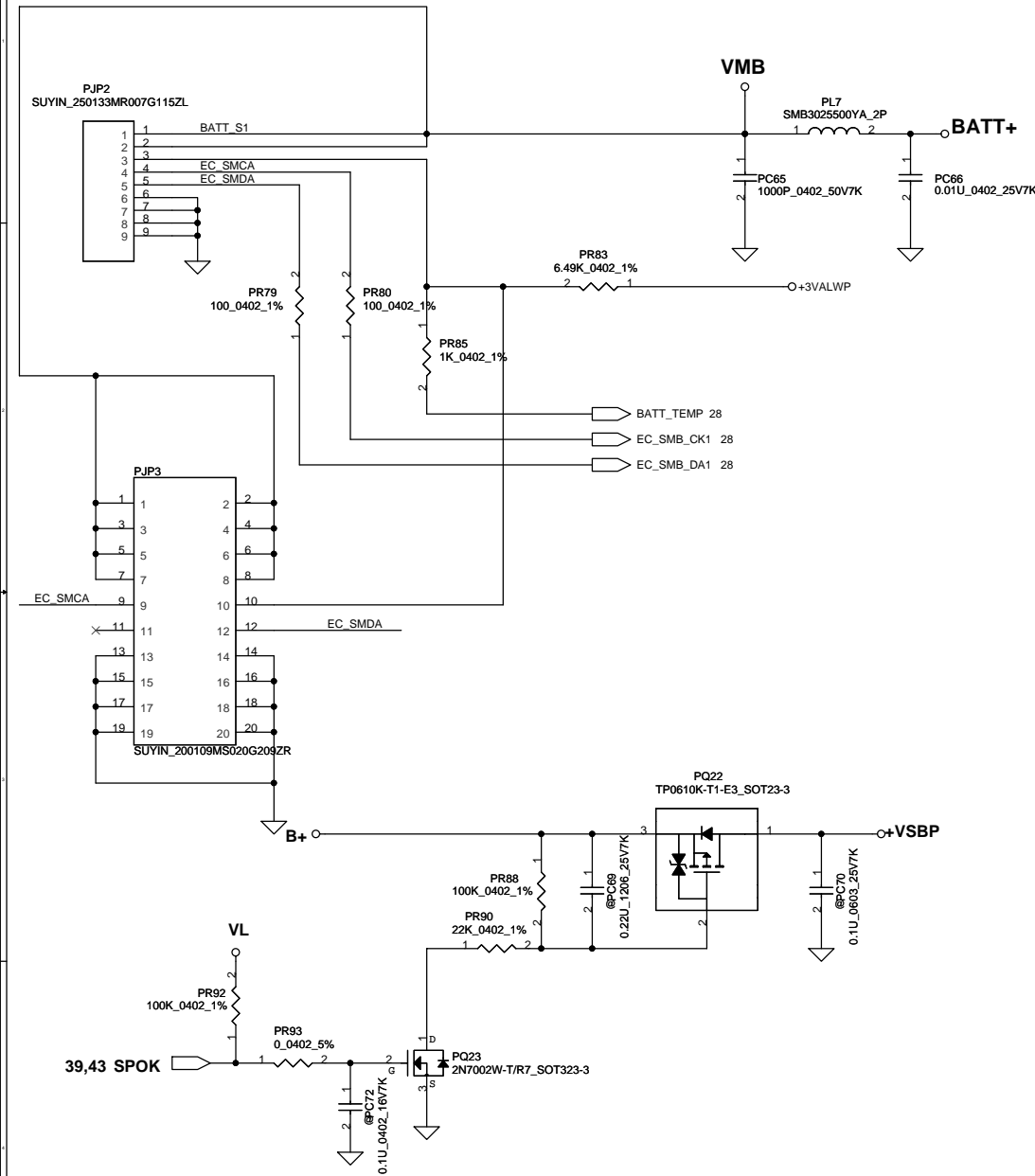
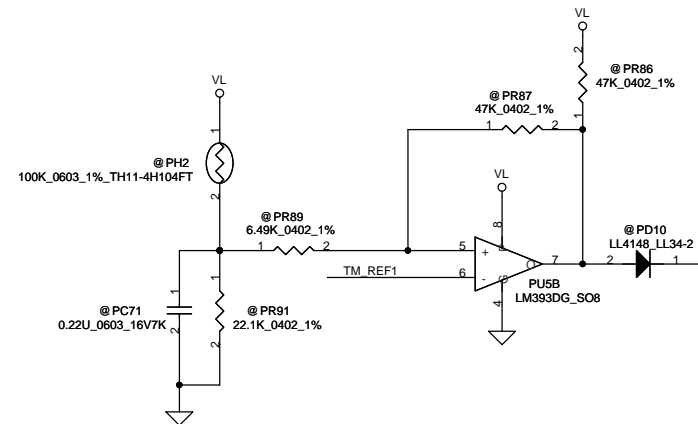
Icharge Setting
 For 2200mA, Icharge=0.8C=0.8*2*2.2=3.52A
 Icharge=(Vsrset/Vdac)*(0.1/PR46)
 IREF=((100k/(100K+17.4K))/3.3)*(0.1/0.02)=Icharge
 IREF=0.7748*Icharge



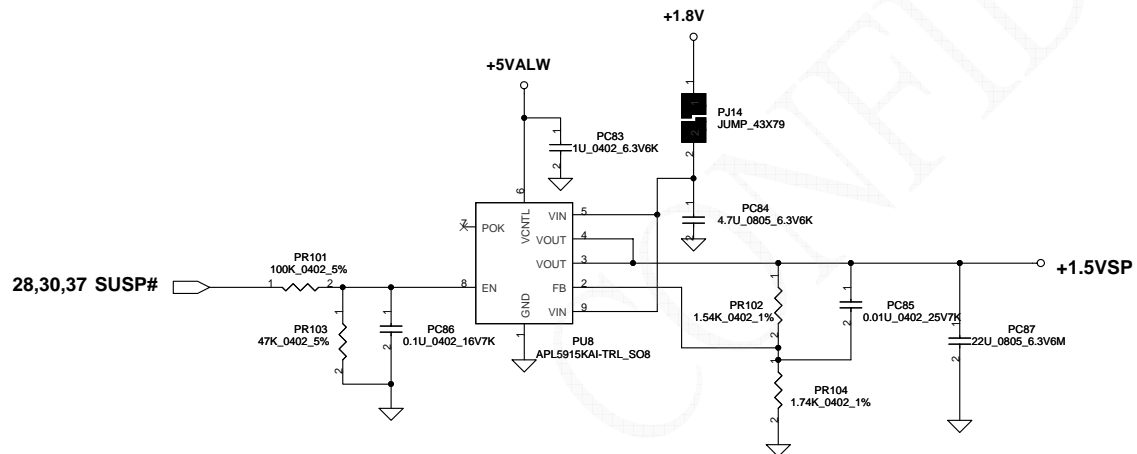
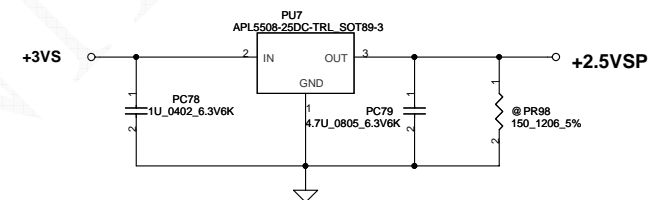
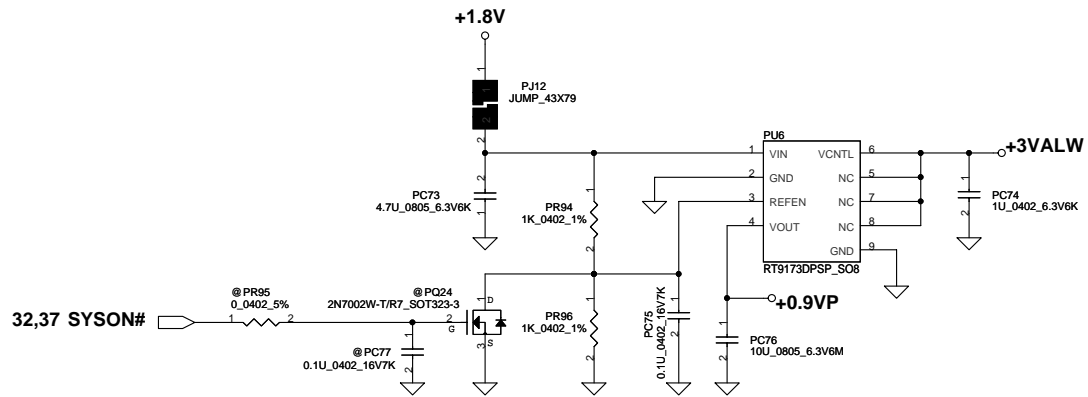
PH1 under CPU botten side :
CPU thermal protection at 92 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 75 degree C



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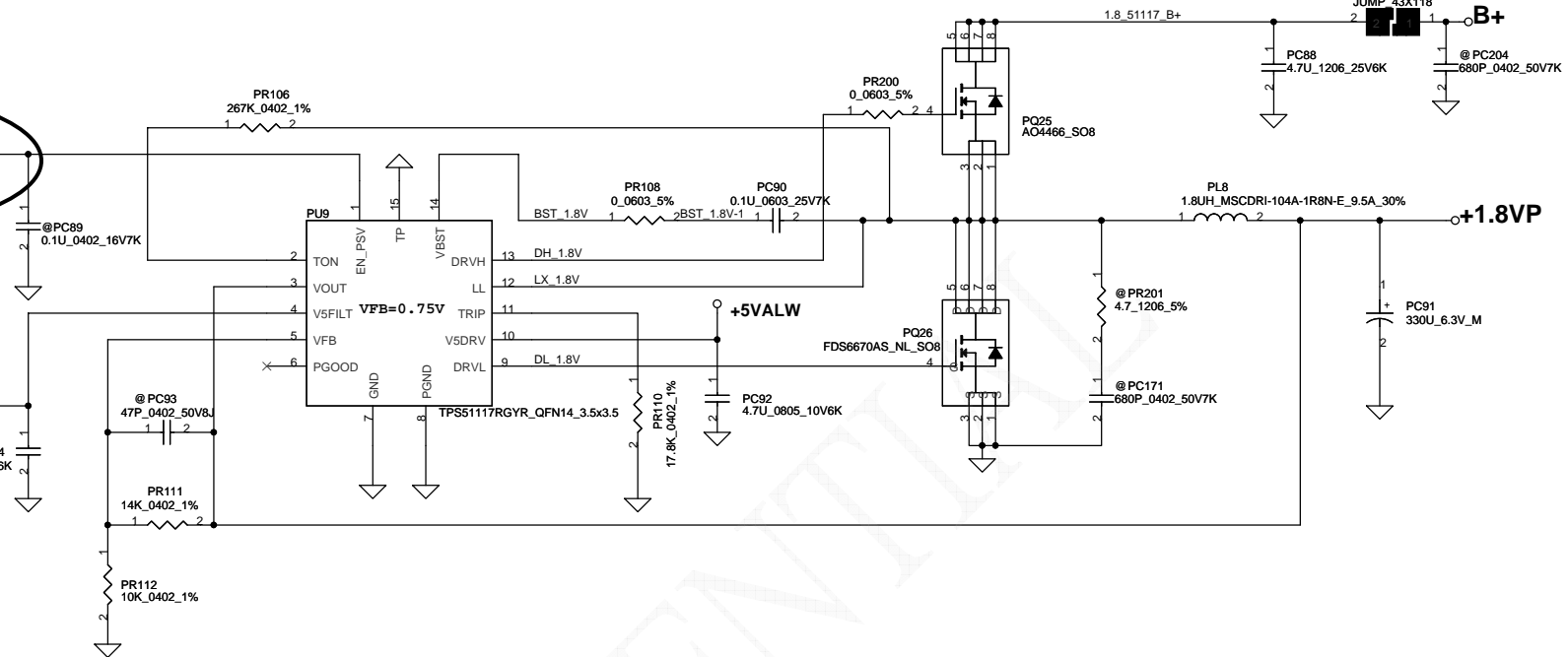
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28,30,37 SYSON

VFB=0.75V
 $V_o = VFB * (1 + PR111 / PR112) = 0.75 * (1 + 14K / 10K) = 1.8V$
 $R_{ton} = 267K \Rightarrow F_{aw} = 297KHz$

Cout ESR=15m ohm
 $I_{peak} = 11.96A$, $I_{max} = 8.372A$, $I_{ocp} = 14.352A$
 $\Delta I = ((19 - 1.8) * (1.8 / 19)) / (L * F_{sw})$
 $((19 - 1.8) * (1.8 / 19)) / (1.8u * 297000) = 3.048A$
 $\Rightarrow 1/2 \Delta I = 1.524A$

$R_{trip} = 17.8K$
 $I_{ocp} = 13.04A - 21.41A$

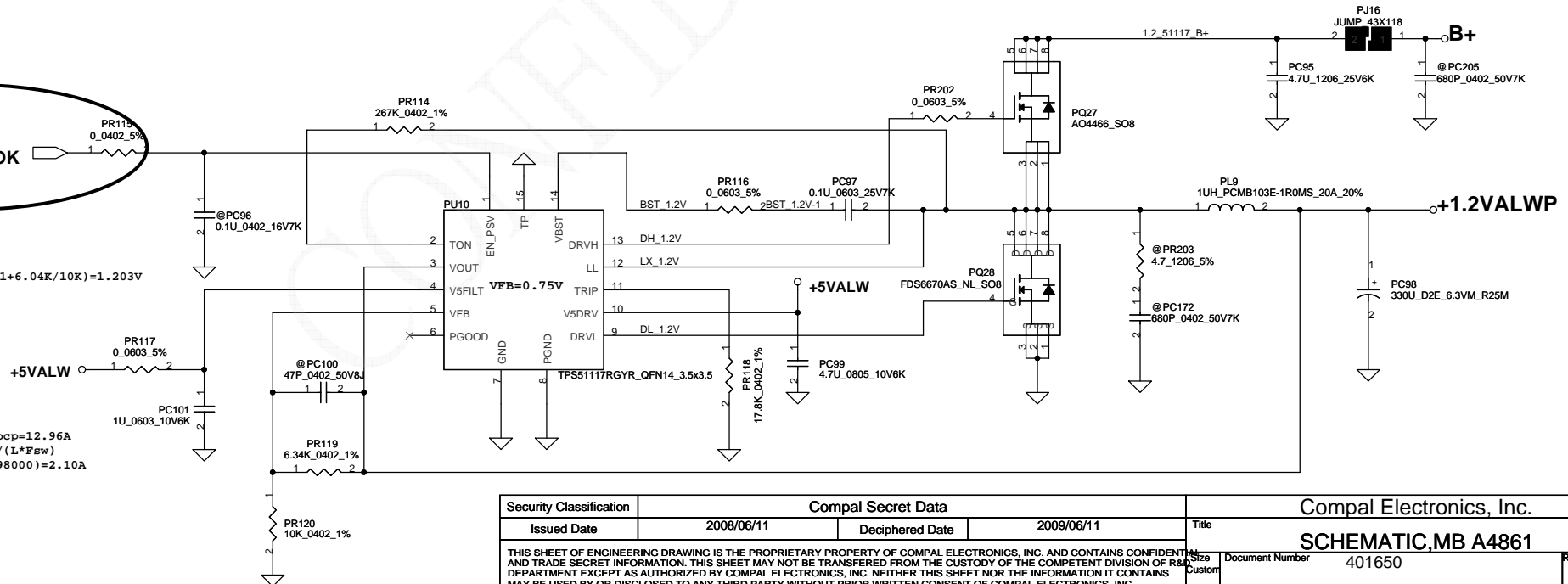


39,41 SPOK

VFB=0.75V
 $V_o = VFB * (1 + PR119 / PR120) = 0.75 * (1 + 6.04K / 10K) = 1.203V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 298KHz$

Cout ESR=15m ohm
 $I_{peak} = 10.80A$, $I_{max} = 7.56A$, $I_{ocp} = 12.96A$
 $\Delta I = ((19 - 1.2) * (1.2 / 19)) / (L * F_{sw})$
 $((19 - 1.2) * (1.2 / 19)) / (1.8u * 298000) = 2.10A$
 $\Rightarrow 1/2 \Delta I = 1.05A$

$R_{trip} = 17.8K$
 $I_{ocp} = 12.75A - 20.83A$



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Version change list (P.I.R. List)

Page 1 of 1
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Customer changed CPU to TF36/38.	TF36/38 is 31W CPU, must change MOS to 1H2L.	0.1	44	Add PQ31 and PQ34 SB000009F80(S TR AO4456 1N SO8)	08, 11/13	to DVT
2	Change CP OCP setting.	TF36/38 CPU OCP setting change.	0.1	44	Change PR198 to SD034402180(S RES 1/16W 4.02K 0402 1%)	08, 11/13	to DVT
3	S3 Mode issue.	Because APL5915 has 0.4V enable voltage, so add PR103 to pull down enable voltage when system in S3 mode	0.1	42	Add PR103 SD028470280(S RES 1/16W 47K 0402 5%)	08, 11/13	to DVT
4	AMD issue.	AMD request add 1.2V to 1.22V for chipset.	0.1	43	Change PR119 from SD034604180 to SD034634180.	08, 11/17	to DVT
5	EMI issue.	EMI request add charger snubber.	0.1	40	Add PR48 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC50 SE074681K80(S CER CAP 680P 50V K X7R 0402)	08, 11/17	to DVT
6	Cost issue.	Cost issue.	0.1	44	Change PC201 from SF000000G80(S ELE CAP 220U 25V M HA0 MVY) to SF22004M210(S ELE CAP 220U 25V M 8X10.2 CE-AX)	08, 11/17	to DVT
7	Support charge voltage.	Support charge voltage.	0.1	40	Delete PQ18 SB000006800(S TR 2N7002W T/R7 1N SOT-323)	08, 11/26	to DVT
8	Support charge voltage.	Support charge voltage.	0.1	40	Delete PQ16 SB923010020(S TR SI2301BDS-T1-E3 1P SOT23)	08, 11/26	to DVT
9	Support charge voltage.	Support charge voltage.	0.1	40	Delete PR66 SD028000080(S RES 1/16W 0 0402 5%)	08, 11/26	to DVT
10	Support charge voltage.	Support charge voltage.	0.1	40	Delete PR69 SD034100380(S RES 1/16W 100K 0402 1%)	08, 11/26	to DVT
11	Support charge voltage.	Support charge voltage.	0.1	40	Delete PC63 SE074102K80(S CER CAP 1000P 50V K X7R 0402)	08, 11/26	to DVT
12	Support charge voltage.	Support charge voltage.	0.1	40	Add PR70 SD034210380(S RES 1/16W 210K 0402 1%)	08, 11/26	to DVT
13	Support charge voltage.	Support charge voltage.	0.1	40	Add PR71 SD034499380(S RES 1/16W 499K 0402 1%)	08, 11/26	to DVT
14							
15							
16							
17							
18							

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Version change list (P.I.R. List) for HW

Item	Reason for change	Modify List	Rev.	PG#	Item	Reason for change	Modify List	Rev.	PG#
1	Material Change	Change U1 to APL5607	DVT	P06	26	Material Change	Change U82 to ALC272X-GR (SA00002CI20)	PVT	P35
2	Material Change	Change U85 to AR8132	DVT	P25	27	Material Change	Change U27 to KB926QFD3 (SA00001J580)	PVT	P28
3	8132 issue, OS black screen	Change L90 to R546 (0_0805)	DVT	P25	28	Material Change	Change U85 to AR8132M-AL1E (SA000034V00)	PVT	P25
4	Circuit issue	Add R677	DVT	P32	29	Material Change	Change U85 to AR8132-AL1E (SA000036Y00)	Pre-PVT	P25
5	RT5159 ID issue	Pop R680 to 0_0402_5%	DVT	P27	30	BOM change	Del D13,D4	Pre-PVT	P06
6	[EMI] Camera co-layout choke	Change R759,R760 to 0_0402 Reserve L77	DVT	P24	31	ESD Cost down	Del D16,D39,D40	Pre-PVT	
7	[Cost Down] audio LDO	Reserve U81 Pop784	DVT	P35	32	ESD Cost down	Change D15 to SCA00000200	Pre-PVT	
8	RT5159 unknow issue	Reserve R548, pop R547	DVT	P27	33	BOM change	Change R251,R253 to 1K	Pre-PVT	
9	[ESD]	Pop D39,D40	DVT	P36					
10	[ESD]	Pop D14,D15	DVT	P36					
11	[ESD]	Pop D16	DVT	P29					
12	[EMI]	Reserve C859 for EMI	DVT	P27					
13	Modify PWR Sequence	Reserve R104,R108 Pop R658,R652	DVT	P34 P28					
14	[EMI]	Reserve C861 for EMI	DVT	P16					
15	Material Change	Change JRJ1 type	DVT	P26					
16	Material Change	Change C924,C971 to 3900pF_0402	DVT	P36					
17	[EMI]	Reserve C350,C352,C353,C354	DVT	P15					
18	[EMI]	Pop R673 to 10ohm_0402 Pop C858 to 10pF_0402	PVT	P27					
19	[EMI]	Pop C859 to 0.1uF_0402	PVT	P27					
20	[EMI]	Pop C350,C352,C353,C354 to 0.1uF_0402	PVT	P15					
21	Material Change	Change R251,R253 to 1.1Kohm Change R250,R252 to 1.2Kohm	PVT	P34					
22	Material Change	Change Y2 footprint to correct	PVT	P18					
23	Material Change	Only cChange R810,R807 P/N to SM010012010	PVT	P36					
24	Circuit Change	Reserve PWN FAN function. Add R247,R40,JP38	PVT	P06					
25	Material Change	Change R814,R815 to 56.2ohm_0402	PVT	P36					

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